UNICMICRO 广芯微电子

UM8G006A

Ultra-low Power 8-bit MCU: 1T8051 Core, 64KB eFlash, 4 KB + 256 B SRAM, 12-bit ADC, Crystal-free / LDO / RC Circuit, Rich Interfaces, Anti-crash, Anti-copy

Product Features

- **Ultra-low power management system**
  - 1.1 μA @ 3.0 V DeepSleep mode with timed wake-up, running at low clock speed, data retention for IO, SRAM and register
  - 0.75 μA @ 3.0 V Stop mode, all clocks stopped, data retention for IO, SRAM and register
  - 80 μA/MHz @ 3.0 VActive mode
  - Built-in ROSC/LDO/POR modules, board-level system requires no crystal oscillator/LDO/reset circuit
- **Processor**
  - 8-bit high-performance 8051 core (1T architecture), 6–12 times faster than standard 8051, with a max. main frequency of 16 MHz
- **Memory**
  - RAM: 256 B Idata, 4 KB Xdata
  - 64 KB eFlash
    - ✓ Sector size: 512 B
  - 1 KB EEPROM
    - ✓ Sector size: 512 B
- **Timers/counters**
  - 3 × 16-bit GTIMERs supporting complementary PWM output with dead-time insertion
  - 1 x 16-bit LPTIMER with PWM output
  - 1 x Watchdog timer (WDT)
- **Clocks**
  - Internal high-speed clock RCH: 16 MHz
  - Internal low-speed clock RCL: 38 kHz
  - External crystal oscillator: 16 MHz (max.)
  - External clock input: 16 MHz (max.)
- **Peripherals**
  - PWM: 11 channels of 16-bit PWM output
  - UART: UART0 / UART1 / UART2 / UART3
  - ADC: 8-channel 12-bit SAR ADC, 1 Msps sampling rate

TSSOP20 (6.5*4.4 mm) QFN20 (3*3 mm)

  - I2C: master/slave mode, 400 kbps (max.)
  - SPI: 1 channel, master/slave mode, Mode 0/1/2/3 protocols, 8 Mbps (max.)
  - GPIO: up to 17 channels, configurable internal pull-up / pull-down
  - BEEPER: buzzer with configurable output frequency and polarity
- **Security**
  - Hardware-level anti-copy board
  - Low-voltage detection (LVD) for supply voltage monitoring
  - Low-voltage reset (LVR) and anti-crash design
  - 16-byte UUID
- **Electrical parameters**
  - Operating voltage: 2.5 V–5.5 V
  - Operating temperature: -40℃–+85℃ (≤ 16 MHz)
  - ESD: 8 kV (HBM)
- **Development support**
  - Built-in Bootloader, supporting download via UART & updating of ISP and IAP applications
  - Complete SDK and EVB HDK
  - Offline programmer and UMP tool
- **Odering information**

Type	Model
64 KB	UM8G006A-F8P7 (TSSOP20) UM8G006A-F8U7 (QFN20)

1 Overview

UM8G006A is a low-power 8-bit IoTP processor developed by Unicmicro based on single-cycle 8051 core. Adopting a unique low-power design technology and with a wide operating voltage of 2.5 V – 5.5 V, the chip integrates 64 KB Flash, SRAM (4 KB + 256 B), 12-bit SAR ADC (1 Msps), as well as universal peripheral communication interfaces such as UART, SPI, I2C, PWM and so on.

With built-in high-speed ROSC, LDO and POR, and no crystal/LDO/reset circuit required for the board-level system, UM8G006A is featured by high integration of resources, high interference immunity, high reliability, low power consumption and minimal peripheral components. It also supports Keil MDK, C language and assembly language for software development.

Applications:

- Industrial IoT terminals
- Smart city, smart home, etc.
- Intelligent sensor terminal applications
- General controller applications such as toy control

2 Functional Block Diagram

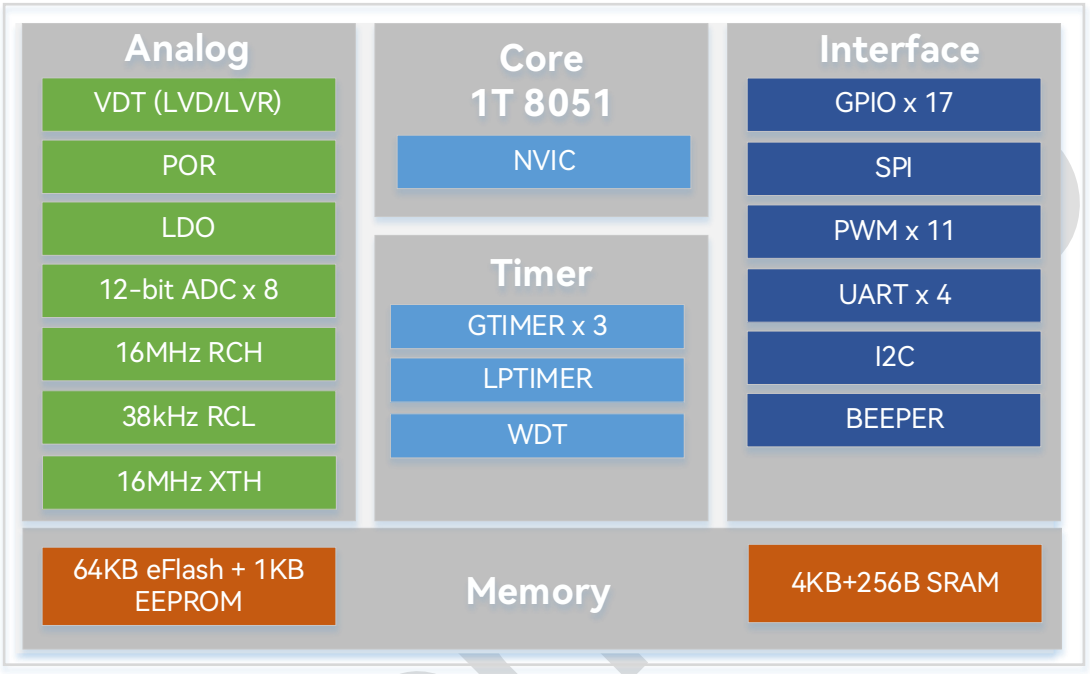


Figure 2-1: Functional Block Diagram

3 Package and Pin Description

3.1 Pinout Diagram

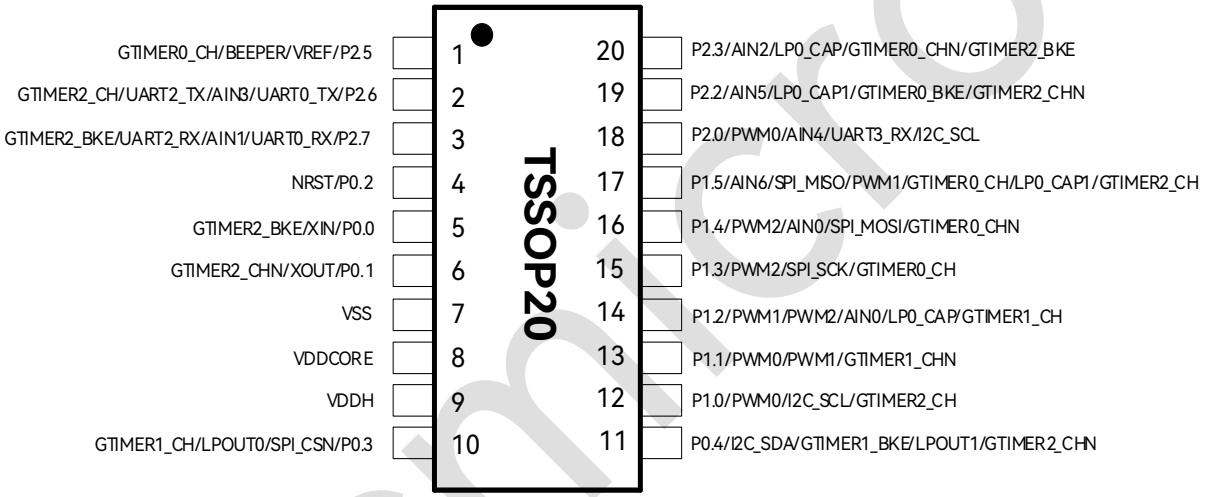


Figure 3-1: UM8G006A-F8P7 (TSSOP20) Pinout Diagram

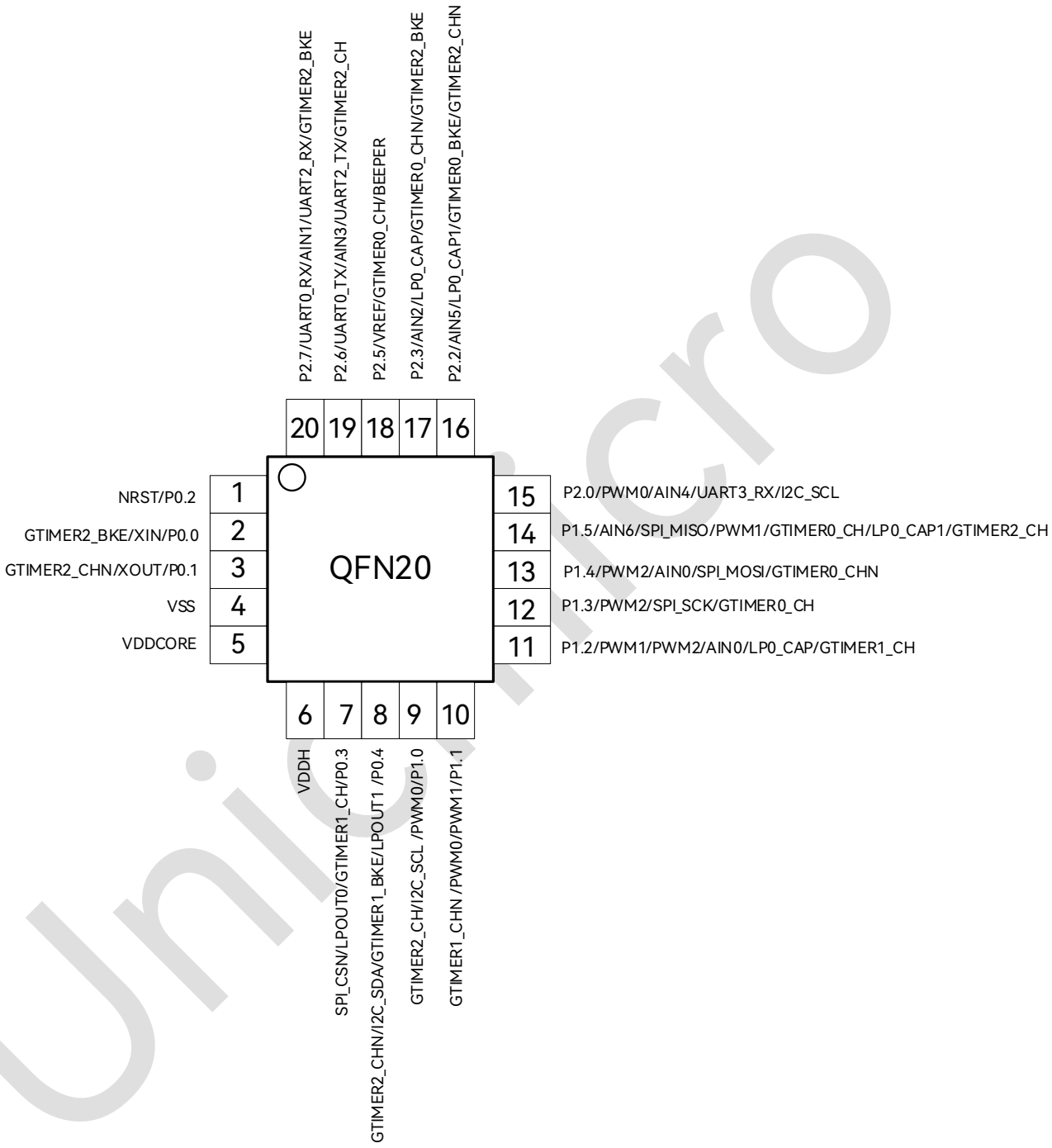


Figure 3-2: UM8G006A-F8P7 (QFN20) Pinout Diagram

3.2 Alternate Function

Table 3-1: Pin Alternate Function

Pin No. in Each Package		Config	Pxx_CFG[2:0]							
TSSOP20	QFN20		0	1	2	3	4	5	6	7
1	18	VREF	P2.5	UART3_TX	SPI_CSN	I2C_SCL	GTIMER0_CH	GTIMER0_BKE	BEEPER	UART0_RX
2	19	AIN3	P2.6	UART0_TX	UART2_TX	SPI_MISO	LPOUT1	GTIMER1_CH	GTIMER2_CH	-
3	20	AIN1	P2.7	UART0_RX	UART2_RX	SPI_MOSI	I2C_SCL	GTIMER1_CHN	GTIMER2_BKE	BEEPER
4	1	NRST/P0.2	-	-	-	-	-	-	-	-
5	2	XIN	P0.0	UART2_RX	SPI_CSN	LPOUT0	GTIMER1_CHN	GTIMER2_BKE	-	-
6	3	XOUT	P0.1	UART2_TX	SPI_SCK	I2C_SDA	LPOUT1	GTIMER0_BKE	GTIMER2_CHN	-
7	4	VSS	-	-	-	-	-	-	-	-
8	5	VDDCORE	-	-	-	-	-	-	-	-
9	6	VDDH	-	-	-	-	-	-	-	-
10	7	LPT_OUT	P0.3	CLKOUT	UART2_TX	UART3_RX	SPI_CSN	LPOUT0	GTIMER1_CH	-
11	8	-	P0.4	UART2_RX	SPI_SCK	I2C_SDA	LPOUT1	GTIMER1_BKE	GTIMER2_CHN	-
12	9	-	P1.0	UART1_RX	UART2_TX	PWM0	I2C_SCL	LP0_IN	GTIMER2_CH	UART2_RX
13	10	-	P1.1	UART1_TX	UART3_RX	PWM1	SPI_MISO	LP0_TRG	GTIMER1_CHN	PWM0 (UART2_TX)
14	11	AIN0	P1.2	UART0_RX	UART3_TX	PWM2	LP0_CAP	GTIMER1_CH	PWM1	-
15	12	-	P1.3	UART0_TX	UART2_RX	SPI_SCK	I2C_SDA	LP0_IN	GTIMER0_CH	PWM2
16	13	AIN0	P1.4	UART1_RX	PWM2	SPI_MOSI	LP0_TRG	GTIMER0_CHN	GTIMER1_BKE	-
17	14	AIN6	P1.5	UART1_TX	PWM1	SPI_MISO	GTIMER0_CH	GTIMER1_BKE	GTIMER2_CH	LP0_CAP1
18	15	AIN4	P2.0	UART3_RX	PWM0	SPI_MOSI	I2C_SCL	LPOUT0	GTIMER0_CHN	-
19	16	AIN5	P2.2	UART3_TX	SPI_CSN	SPI_MISO	I2C_SDA	GTIMER0_BKE	GTIMER2_CHN	LP0_CAP1
20	17	AIN2	P2.3	UART3_RX	SPI_SCK	SPI_MOSI	LP0_CAP	GTIMER0_CHN	GTIMER2_BKE	-

3.3 Pin Description

Table 3-2: Pin Description

Pin No. in Each Package		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP20	QFN20			DIR	PU PD		
1	18	P2.5	I/O	HZ	-	P2.5 (default)	General-purpose digital input/output pin
						BEEPER	Beeper output signal
						VREF	V_{REF} input of ADC
						UART0_RX	RX signal of UART0
						UART3_TX	TX signal of UART3
						SPI_CSN	CS signal of SPI
						I2C_SCL	SCL signal of I2C
						GTIMER0_CH	Capture and PWM signals of GTIMER0
						GTIMER0_BKE	Break signal of GTIMER0
2	19	P2.6	I/O	HZ	-	P2.6 (default)	General-purpose digital input/output pin
						UART0_TX	TX signal of UART0
						AIN3	CH3 signal of ADC
						UART2_TX	TX signal of UART2 (for download via BOOT UART, and shall be used with NRST signal.)
						SPI_MISO	MISO signal of SPI
						LPOUT1	PWM1 signal of LPTIMER
						GTIMER1_CH	Capture and PWM signals of GTIMER1
						GTIMER2_CH	Capture and PWM signals of GTIMER2
3	20	P2.7	I/O	DI	-	P2.7 (default)	General-purpose digital input/output pin
						UART0_RX	RX signal of UART0
						AIN1	CH1 signal of ADC

Pin No. in Each Package		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP20	QFN20			DIR	PU PD		
						UART2_RX	RX signal of UART2 (for download via BOOT UART, and shall be used with NRST signal.)
						SPI_MOSI	MOSI signal of SPI
						I2C_SCL	SCL signal of I2C
						GTIMER1_CHN	PWM reverse signal of GTIMER1
						GTIMER2_BKE	Break signal of GTIMER2
						BEEPER	Beeper signal
4	1	P0.2	I/O	DI	PU	NRST (default)	Reset pin for low-level reset and internal forced pull-up. This signal is necessary for batch download via UART, it is recommended to access this pin signal (pad or pin) onto PCB.
						P0.2	General-purpose digital input/output pin
5	2	P0.0	I/O	HZ	-	P0.0 (default)	General-purpose digital input/output pin
						XIN	Crystal oscillator input pin
						UART2_RX	RX signal of UART2
						SPI_CSN	CS signal of SPI
						LPOUT0	PWM0 signal of LPTIMER
						GTIMER1_CHN	PWM reverse signal of GTIMER1
						GTIMER2_BKE	Break signal of GTIMER2
6	3	P0.1	I/O	HZ	-	P0.1 (default)	General-purpose digital input/output pin
						XOUT	Crystal oscillator output pin
						UART2_TX	TX signal of UART2
						SPI_SCK	SCK signal of SPI
						I2C_SDA	SDA signal of I2C

Pin No. in Each Package		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP20	QFN20			DIR	PU PD		
						LPOUT1	PWM1 signal of LPTIMER
						GTIMER0_BKE	Break signal of GTIMER0
						GTIMER2_CHN	PWM reverse signal of GTIMER2
7	4	VSS	G	AP	-	VSS	Power ground
8	5	VDDCORE	P	AP	-	VDDCORE	Internal LDO output (1 μF capacitor required)
9	6	VDDH	P	AP	-	V_{DDH}	Chip supply 2.5 V–5.5 V
10	7	P0.3	I/O	HZ	-	P0.3 (default)	General-purpose digital input/output pin
						LPT_OUT	Output signal of LPTIMER
						CLKOUT	Output signal of clock
						UART2_TX	TX signal of UART2
						UART3_RX	RX signal of UART3
						SPI_CSN	CS signal of SPI
						LPOUT0	PWM0 signal of LPTIMER
						GTIMER1_CH	Capture and PWM signals of GTIMER1
11	8	P0.4	I/O	HZ	-	P0.4 (default)	General-purpose digital input/output pin
						UART2_RX	RX signal of UART2
						SPI_SCK	SCK signal of SPI
						I2C_SDA	SDA signal of I2C
						LPOUT1	PWM1 signal of LPTIMER
						GTIMER1_BKE	Break signal of GTIMER1
						GTIMER2_CHN	PWM reverse signal of GTIMER2
12	9	P1.0	I/O	DI	-	P1.0 (default)	General-purpose digital input/output pin
						PWM0	PWM0 signal
						LP0_IN	LPTIMER input signal
						I2C_SCL	SCL signal of I2C
						UART1_RX	RX signal of UART1

Pin No. in Each Package		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP20	QFN20			DIR	PU PD		
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						GTIMER2_CH	Capture and PWM signals of GTIMER2
13	10	P1.1	I/O	HZ	-	P1.1 (default)	General-purpose digital input/output pin
						PWM0	PWM0 signal
						PWM1	PWM1 signal
						UART1_TX	TX signal of UART1
						UART3_RX	RX signal of UART3
						SPI_MISO	MISO signal of SPI
						LP0_TRG	Trigger signal of LPTIMER
						GTIMER1_CHN	PWM reverse signal of GTIMER1
						UART2_TX	TX signal of UART2
14	11	P1.2	I/O	DI	-	P1.2 (default)	General-purpose digital input/output pin
						PWM2	PWM2 signal
						AIN0	CH0 signal of ADC
						PWM1	PWM1 signal
						UART0_RX	RX signal of UART0
						UART3_TX	TX signal of UART3
						LP0_CAP	Capture signal of LPTIMER
						GTIMER1_CH	Capture and PWM signals of GTIMER1
15	12	P1.3	I/O	HZ	-	P1.3 (default)	General-purpose digital input/output pin
						UART0_TX	TX signal of UART0
						PWM2	PWM2 signal
						UART2_RX	RX signal of UART2
						SPI_SCK	SCK signal of SPI
						I2C_SDA	SDA signal of I2C
						LP0_IN	LPTIMER input signal

Pin No. in Each Package		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP20	QFN20			DIR	PU PD		
						GTIMER0_CH	Capture and PWM signals of GTIMER0
16	13	P1.4	I/O	HZ	-	P1.4 (default)	General-purpose digital input/output pin
						UART1_RX	RX signal of UART1
						AIN0	CH0 signal of ADC
						SPI_MOSI	MOSI signal of SPI
						PWM2	PWM2 signal
						LP0_TRG	Trigger signal of LPTIMER0
						GTIMER0_CHN	PWM reverse signal of GTIMER0
						GTIMER1_BKE	Break signal of GTIMER1
17	14	P1.5	I/O	HZ	-	P1.5 (default)	General-purpose digital input/output pin
						UART1_TX	TX signal of UART1
						SPI_MISO	MISO signal of SPI
						AIN6	CH6 signal of ADC
						PWM1	PWM1 signal
						GTIMER0_CH	Capture and PWM signals of GTIMER0
						GTIMER1_BKE	Break signal of GTIMER1
						GTIMER2_CH	Capture and PWM signals of GTIMER2
						LP0_CAP1	Capture1 signal of LPTIMER
18	15	P2.0	I/O	HZ	-	P2.0 (default)	General-purpose digital input/output pin
						AIN4	CH4 signal of ADC
						UART3_RX	RX signal of UART3
						PWM0	PWM0 signal
						SPI_MOSI	MOSI signal of SPI
						I2C_SCL	I2C_SCL
						LPOUT0	PWM0 signal of LPTIMER

Pin No. in Each Package		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP20	QFN20			DIR	PU PD		
						GTIMER0_CHN	PWM reverse signal of GTIMER0
19	16	P2.2	I/O	HZ	-	P2.2 (default)	General-purpose digital input/output pin
						AIN5	CH5 signal of ADC
						UART3_TX	TX signal of UART3
						SPI_CSN	CS signal of SPI
						SPI_MISO	MISO signal of SPI
						I2C_SDA	SDA signal of I2C
						GTIMER0_BKE	Break signal of GTIMER0
						GTIMER2_CHN	PWM reverse signal of GTIMER2
						LP0_CAP1	Capture1 signal of LPTIMER
20	17	P2.3	I/O	HZ	-	P2.3 (default)	General-purpose digital input/output pin
						AIN2	CH2 signal of ADC
						UART3_RX	RX signal of UART3
						SPI_SCK	SCK signal of SPI
						SPI_MOSI	MOSI signal of SPI
						LP0_CAP	Capture signal of LPTIMER
						GTIMER0_CHN	PWM reverse signal of GTIMER0
						GTIMER2_BKE	Break signal of GTIMER2

Notes:

A—analog signal; D—digital signal; I—input; O—output; G—ground; P—power; PU—pull up; PD—pull down; HZ—high impedance state.

4 Electrical Parameters

4.1 Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1: Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
V_{SS}	External supply voltage	-0.3	-	V
V_{DDH}		-	+6.0	V
T_{stg}	Storage temperature	-55	+150	℃
T_J	Junction temperature	-40	+105	℃
I_{DD}	Max. input current of V_{DDH} pin	-	50	mA
I_{SS}	Max. output current of V_{SS} pin	-	50	mA
$V_{ESD(HBM)}$	ESD protection voltage	-8	+8	kV

Note: The input voltage of IO pin shall not exceed V_{DDH}, otherwise the chip will be damaged.

4.2 Operating Condition

4.2.1 General Operating Condition

Table 4-2: General Operating Condition

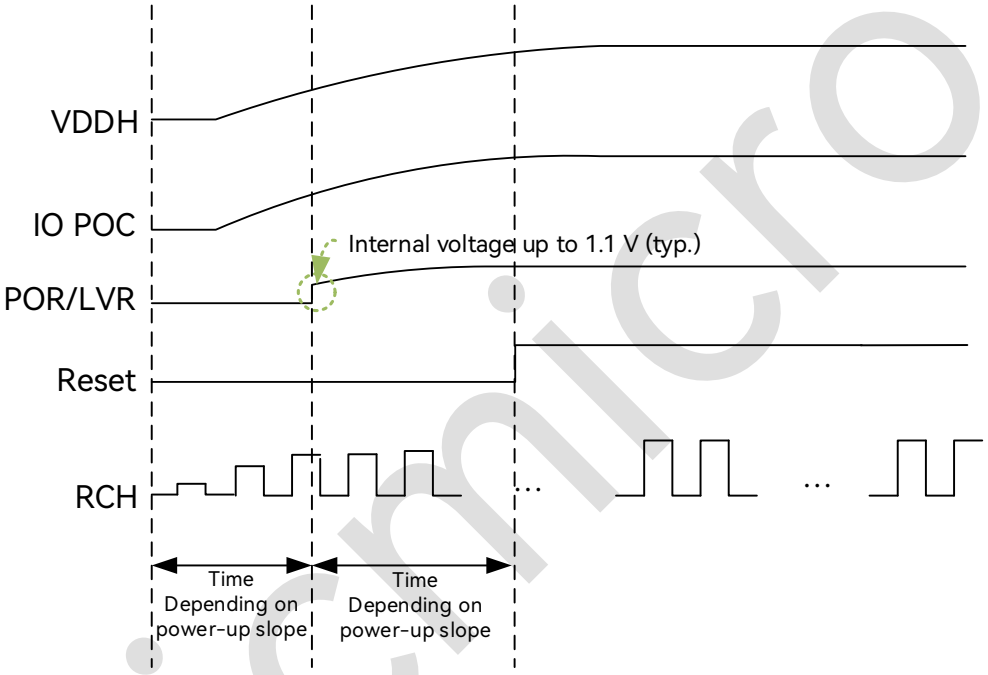
Symbol	Description	Min.	Max.	Unit
V_{DDH}	Operating voltage	2.5	5.5	V
T_A	Ambient temperature	-40	+85	℃
f_{sys}	System frequency	0.1	16	MHz

Note: If f_{sys} is lower than 2 MHz, Flash can only fetch and execute code, but cannot erase or write.

4.2.2 Operating Condition at Power-up / Power-down

Table 4-3: Operating Condition at Power-up / Power-down

Symbol	Description	Min.	Max.	Unit
t_{VDDH}	V_{DDH} rise time rate	0	110,000	μs/V
	V_{DDH} fall time rate	0	110,000	



Note: In the case of low-voltage reset occurs during power-down, the whole power-up process shall be experienced after powering up again.

4.2.3 DC Parameter

- Static parameters (applicable temperature range: T_A = -40℃ – +85℃)

Table 4-4: Static Parameters

Symbol	Description	Test Condition	Min.	Typ.	Max.	Unit
V_{DDH}	Analog supply voltage	Power supply for I/O buffer and pre-driver	2.5	3.3	5.5	V
V_{DDCORE}	Internal LDO voltage temperature drift	25℃	-0.5	-	+0.5	%
		-15℃–+65℃	-5	-	+5	%
		T_A	-10	-	+10	%

Symbol	Description	Test Condition		Min.	Typ.	Max.	Unit
I_{DD}	Operating current	Active mode: V_{DDH} = 3.3 V, T_A = 25 °C; all peripherals are disabled, the code runs "while(1){}" in Flash. CCLK = 16 MHz		-	1.28	-	mA
		Active mode: V_{DDH} = 3.3 V/5 V, T_A = 25 °C; peripherals are enabled, the code runs "while(1){}" in Flash.	CCLK = 16 MHz	-	1.5	-	mA
			CCLK = 4 MHz	-	0.5	0.65	mA
			CCLK = 2 MHz	-	0.3	-	mA
		Sleep mode: V_{DDH} = 3.3 V, T_A = 25 °C		-	0.24	-	mA
		DeepSleep mode: V_{DDH} = 3.3 V; T_A = 25°C		-	1.1	-	μA
		Stop mode: V_{DDH} = 3.3 V; T_A = 25°C		-	0.75	-	μA

Note: The measured value of V_{DDCORE} can be read via Read Vcap.

- **IO Characteristics**

Table 4-5: IO Characteristics

Symbol	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{IL}	Logic low level input current	V_I = 0 V	-1	-	-	μA
I_{IH}	Logic high level input current	$V_I = V_{DD}$	-	-	+1	μA
V_O	Output voltage	Output pin being active	0	-	V_{DD}	V
V_{IH}	Logic high level input voltage	-	0.7 * V_{DDH}	-	-	V
V_{IL}	Logic low level input voltage	-	-	-	0.3 * V_{DDH}	V
V_{hys}	Hysteresis voltage	-	0.1 * V_{DD}	-	-	V
V_{OH}	Logic high level output voltage	5 V, normal output of I_{Load} = 16 mA in high-drive mode and I_{Load} = 8 mA in low-drive mode.	V_{DDH} - 0.3	-	-	V

Symbol	Description	Test Condition	Min.	Typ.	Max.	Unit
		3.3 V, normal output of I_{Load} = 8 mA in high-drive mode and I_{Load} = 4 mA in low-drive mode.	2.4	-	-	V
V_{OL}	Logic low level output voltage	5 V, normal output of I_{Load} = 16 mA in high-drive mode and I_{Load} = 8 mA in low-drive mode.	-	-	0.5	V
		3.3 V, normal output of I_{Load} = 8 mA in high-drive mode and I_{Load} = 4 mA in low-drive mode.	-	-	0.4	V
I_{OH}	Logic high level output current	5 V, normal output in high-drive mode normal output in low-drive mode	16 8	- -	- -	mA
		3.3 V, normal output in high-drive mode normal output in low-drive mode	8 4	- -	- -	mA
I_{OL}	Logic low level output current	5 V, normal output in high-drive mode normal output in low-drive mode	16 8	- -	- -	mA
		3.3 V, normal output in high-drive mode normal output in low-drive mode	8 4	- -	- -	mA
R_{pup} R_{pdn}	Pull up / down current	5 V / 3.3 V	20	60	100	kΩ
C_{IN}	Capacitive impedance	5 V / 3.3 V	-	-	10	pF

4.2.4 Internal RCH Oscillator

Unless otherwise specified, V_{DDH} = 5.0 V, T_A = -40℃–85℃.

Table 4-6: RCH Oscillator Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{HSI}	Clock frequency	T_A = -40℃–85℃	16 * (1 - 2.5%)	16	16 * (1 + 2.5%)	MHz

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Duty	Duty cycle	f_{HSI} = 16 MHz	45	50	55	%
t_{SU}	Clock setup time	-	-	1.2	-	μs
I_{VDD}	Current consumption	-	-	80	120	μA

4.2.5 Internal RCL Oscillator

Unless otherwise specified, V_{DDH} = 5.0 V, T_A = -40℃~85℃.

Table 4-7: RCL Oscillator Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{LSI}	Clock frequency	-	38 * (1 - 10%)	38	38 * (1 + 10%)	kHz
Duty	Duty cycle	-	45	50	55	%
t_{SU}	Clock setup time	-	-	100	200	μs
I_{VDD}	Current consumption	-	-	260	500	nA

4.2.6 External Crystal Oscillator XTH

Unless otherwise specified, V_{DDH} = 5.0 V, T_A = -40℃~85℃.

Table 4-8: XTH Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{OSC_IN}	Frequency range	-	2.0	16	24	MHz
t_{SU}	Clock setup time	-	-	2	-	ms
I_{VDD}	Current consumption	-	-	0.9	-	mA
I_{lk}	Leakage current	-	-	0.01	0.02	μA

4.2.7 VDT Voltage Detection (LVR/LVD)

Unless otherwise specified, V_{DDH} = 5.0 V, T_A = -40~85℃.

Table 4-9: Low Voltage Detection (LVR) Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{IN_LVR}	Input detection voltage range	-	0	-	V_{DD}	V
V_{LVR}	Detection threshold	Deepsleep mode	-	0.9	-	V
		Active mode	-	1.1	-	V
V_{HYS}	Hysteresis voltage	-	-	100	-	mV

Table 4-10: Low Voltage Detection (LVD) Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{IN_LVD}	Input detection voltage range	-	0	-	V_{DD}	V
V_{LVD}	Detection threshold	ADJ_LVD<3:1>=000	-	4.39	-	V
		ADJ_LVD<3:1>=001		3.95		
		ADJ_LVD<3:1>=010		3.59		
		ADJ_LVD<3:1>=011		3.29		
		ADJ_LVD<3:1>=100		3.04		
		ADJ_LVD<3:1>=101		2.82		
		ADJ_LVD<3:1>=110		2.63		
		ADJ_LVD<3:1>=111		2.46		
V_{HYS}	Hysteresis voltage	-	-	100	-	mV

4.2.8 Memory Characteristics

Unless otherwise specified, V_{DDH} = 5.0 V, T_A = -40℃~85℃.

Table 4-11: eFlash Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
ECflash	Sector endurance	-	20 K	-	-	cycles
RETflash	Data retention	-	10	-	-	year
t_{prog}	Program time	16 MHz	-	-	50	μs
		4 MHz	-	-	70	μs
t_{erase}	Sector erase time	16 MHz	-	-	18	ms
		4 MHz	-	-	19	ms
I_{read}	Read current	16 MHz	-	1.2	1.3	mA
		4 MHz	-	0.3	0.4	mA
I_{erase}	Sector erase current	-	-	0.4	0.5	mA
$I_{program}$	Program current	-	-	0.4	0.5	mA

Table 4-12: EEPROM Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
ECflash	Sector endurance	-	20 K	-	-	cycles
RETflash	Data retention	-	10	-	-	year
t_{prog}	Program time	16 MHz	-	-	50	μs
		4 MHz	-	-	70	μs
t_{erase}	Sector erase time	16 MHz	-	-	18	ms
		4 MHz	-	-	19	ms

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
I_{read}	Read current	16 MHz	-	1.2	1.3	mA
		4 MHz	-	0.3	0.4	mA
I_{erase}	Sector erase current	-	-	0.4	0.5	mA
$I_{program}$	Program current	-	-	0.4	0.5	mA

4.2.9 ESD/Latchup Characteristics

All the data below are measured at T_A = +25℃ based on ESDA/JEDEC standard.

Table 4-13: ESD/Latchup Characteristics

Symbol	Description	Class	Max.	Unit
$V_{ESD(HBM)}$	ESD @ Human Body Mode	Class 3B	8000	V
$V_{ESD(CDM)}$	ESD @ Charge Device Mode	Class C2	500	V
$I_{latchup}$	Latch up current	Class IA	200	mA

4.2.10 ADC Characteristics

The following electrical characteristics are measured at T_A = 25℃, V_{DDH} = 3.3 V and V_{DDD25} = 2.5 V.

Table 4-14: ADC Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{ADCIN}	Input voltage range	Single ended	0	-	V_{DD}	V
V_{REF}	ADC reference voltage	-	-	V_{DD}	-	V
I_{ADC}	-	-	0.7	0.9	1.2	mA
C_{ADCIN}	ADC input capacitance	-	3.5	4	4.5	pF
f_{ADCCLK}	ADC clock frequency	-	0.5	4	16	MHz
$t_{ADCSTART}$	Startup time of ADC bias current	-	2	3	4	μs
t_{ADC}	ADC capture and conversion time	-	16	16	16	cycle
ENOB	-	-	9.5	10	10.4	bit
DNL	Differential non-linearity	-	-2	±1	2	LSB
INL	Integral non-linearity	-	-3	±1	3	LSB
E_o	Offset error	-	-2	±1	2	LSB
E_g	Gain error	-	-2	±1	2	LSB
$t_{capture}$	ADC capture time	-	4	4	4	cycle
$t_{convison}$	ADC conversion time	-	12	12	12	cycle

Note: Not tested in production.

4.2.11 Wakeup Time from Low-power Mode

Table 4-15: Wakeup Time from Low-power Mode

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
t_{wakeup}	Wakeup time from DeepSleep mode to Active mode	Regulator voltage = 2.5 V, T_A = 25℃, 16MHz	12.0	16.6	18.0	μs

4.3 Power Supply Scheme

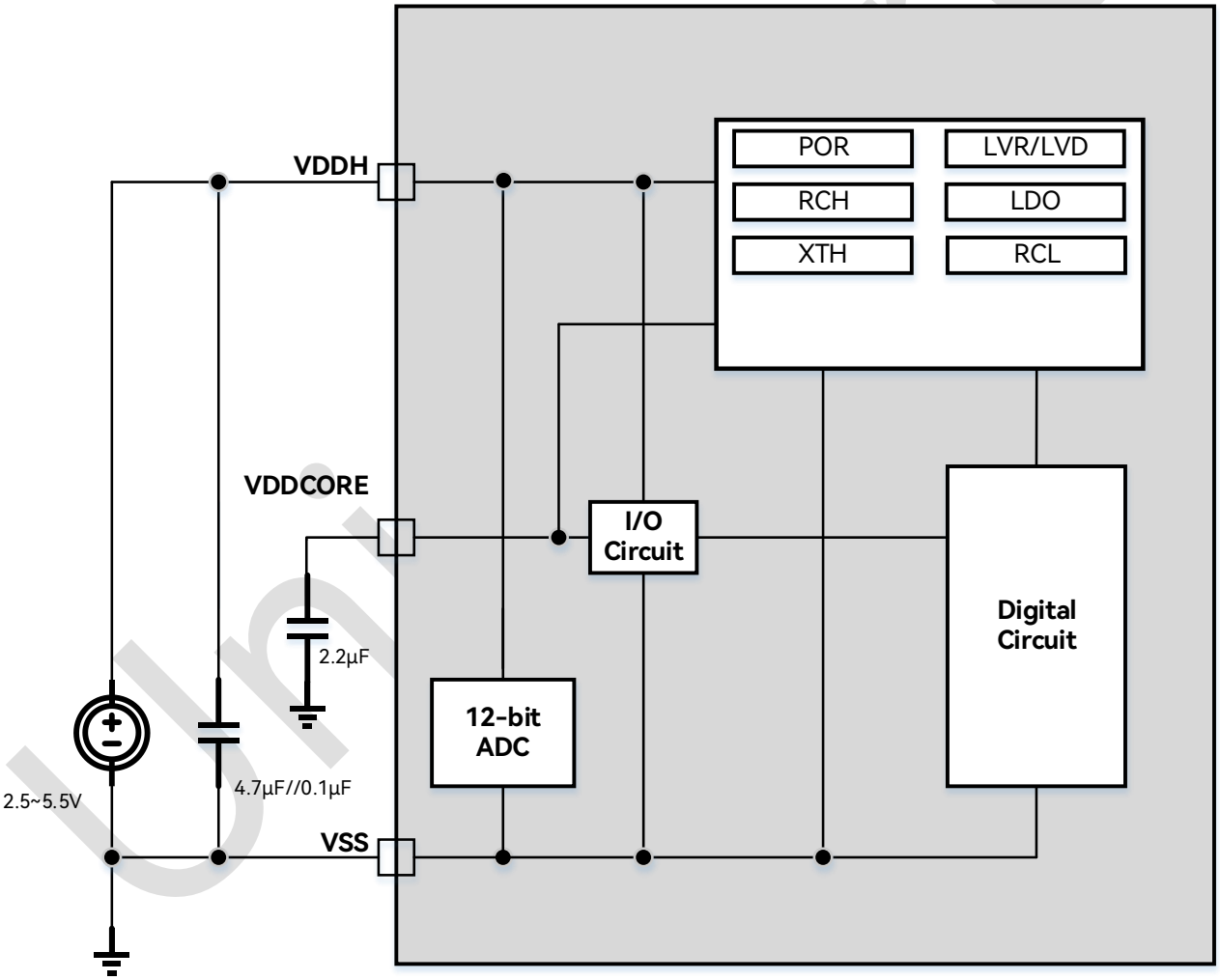


Figure 4-1: Power Supply Scheme

5 ADC

5.1 Main Features

- 12-bit resolution
- Reference voltage: V_{DDA} or external V_{REF}
- Up to 8 analog channel inputs, with channels 0–6 as external inputs and channel 7 input source fixed as internal LDO
- Sampling rate: 1 Msps
- ADC supply/reference source configurable as V_{DDH} or external V_{REF} (when configured to 1, pin P2_5 serves as the external reference input)

5.2 Functional Block Diagram

When P1.2 and P1.4 function as ADC channels, they will pass through an Analog Mux before entering analog-to-digital sampling, which will lead to some characteristics differences between the channel and other ADC channels.

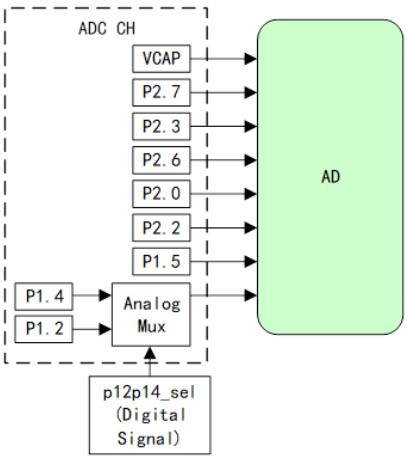


Figure 5-1: ADC Functional Block Diagram

6 UART0/1/2/3

6.1 UART0/1

- UART0 supports four operating modes.
- UART1 supports two operating modes.

6.1.1 UART0 Operating Mode

UART0 supports four operating modes. Before communication, the user must initialize the relevant registers and select the appropriate operating mode and baud rate. Different operating modes can be selected by setting SM0/SM1.

Table 6-1: List of UART0 Operating Mode

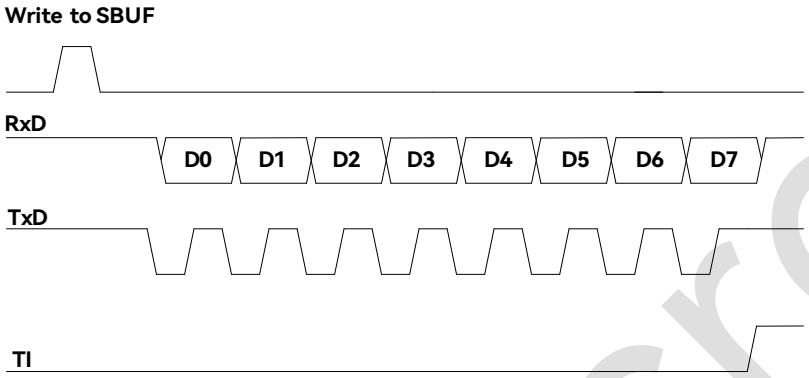
SM0	SM1	Mode	Description	Baud Rate
0	0	0	Shift register	SYSCLK / 12
0	1	1	8-bit UART	Configurable
1	0	2	9-bit UART	SYSCLK / 16
1	1	3	9-bit UART	Configurable

- Mode 0: synchronous, half-duplex communication

  Mode 0 supports synchronous communication with external devices. Serial data is transmitted and received on the RX pin, while the shift clock is transmitted via the TX pin. In this mode, 8 bits are transmitted and received per frame, with the least significant bit (LSB) received or transmitted first.

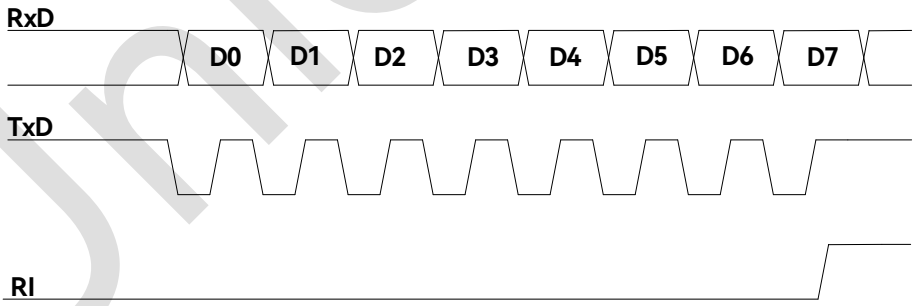
  Any write operation targeting the SBUF register initiates transmission, and the TX control block starts shifting out data on the next system clock. Data conversion occurs on the falling edge of

the shift clock; the contents of the shift register shift leftward one bit at a time, with the null bit set as 0. Upon completion of transmission, the TX control block stops transmitting and then sets TI on the rising edge of the next system clock.



Transmit Timing of Mode 0

Initialize reception by setting REN to 1 and clearing RI to 0. Data is latched on the rising edge of the shift clock, and the contents of the receive shift register are shifted leftward bit by bit. As all 8 bits of data have been shifted into the shift register, the RX control module stops receiving, RI is set on the rising edge of the next system clock, and subsequent reception is allowed only after software clears it.

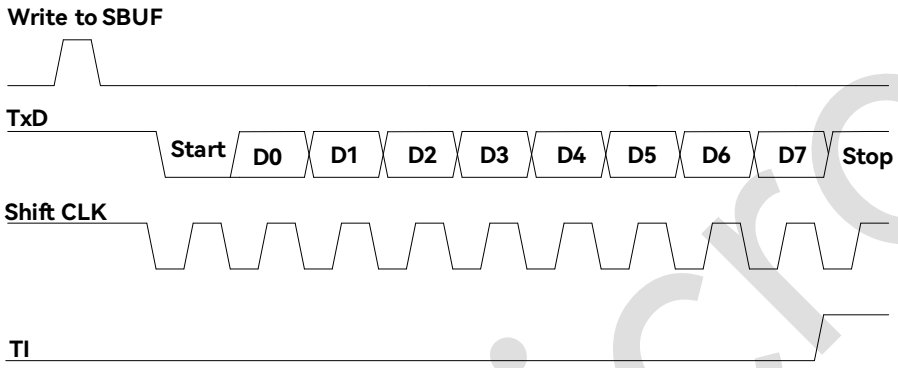


Receive Timing of Mode 0

- Mode 1: 8-bit UART, variable baud rate, asynchronous full-duplex

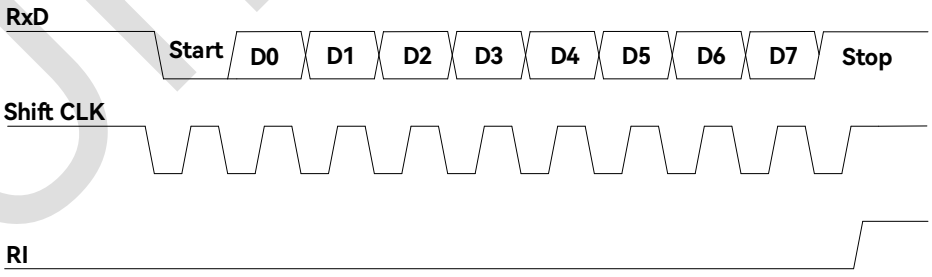
Mode 1 supports 10-bit full-duplex asynchronous communication. The 10 bits consists of one start bit (logic 0), eight data bits (LSB first), and one stop bit (logic 1). During reception, the 8 data bits are stored in SBUF, and the stop bit is stored in RB8.

Any write operation targeting the SBUF register initiates transmission, with the start bit first shifted out on the TX pin, followed by the 8 data bits. After all 8 data bits in the transmit shift register are transmitted, the stop bit is shifted out on the TX pin, and the TI flag is set to issue an interrupt request at the same time as the stop bit is transmitted.



Transmit Timing of Mode 1

Reception is allowed only when REN is set. The serial port starts receiving serial data when the RX pin detects a falling edge. If the start bit is valid, it is shifted into the shift register, followed by the subsequent bits. After the 8 data bits and 1 stop bit are shifted in, the contents of the shift register are loaded into SBUF and RB8 respectively, and then RI is set. At this point, the receiver continues to detect the next falling edge on RX pin. The user shall clear RI by software before resuming reception.



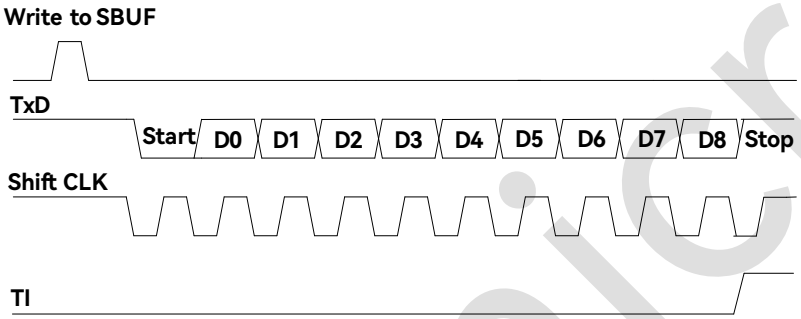
Receive Timing of Mode 1

- Mode 2: 9-bit UART, fixed baud rate, asynchronous full-duplex

Mode 2 supports 11-bit full-duplex asynchronous communication with a fixed baud rate of 1/16 of the system clock. A frame consists of one start bit (logic 0), eight data bits (LSB first), one

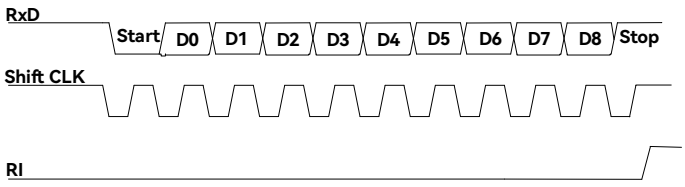
programmable 9th bit, and one stop bit (logic 1). Mode 2 and Mode 3 support multi-machine communication.

Any write operation targeting the SBUF register initiates transmission, and TB8 is loaded into bit 9 of the transmit shift register simultaneously. The start bit is first shifted out on the TX pin, followed by the 9 data bits. After all the data are transmitted, the stop bit is shifted out on the TX pin, and the TI flag is set to issue an interrupt request as the stop bit starts to be transmitted.



Transmit Timing of Mode 2

Reception is allowed only when REN is set. The serial port starts receiving serial data when the RX pin detects a falling edge. If the start bit is valid, it is shifted into the shift register, followed by the subsequent bits. After the 9 data bits and 1 stop bit are shifted in, the contents of the shift register are loaded into SBUF and RB8 respectively, and then RI is set. At this point, the receiver continues to detect the next falling edge on RX pin. The user shall clear RI by software before resuming reception.



Receive Timing of Mode 2

- Mode 3: 9-bit UART, variable baud rate, asynchronous full-duplex

  Mode 3 adopts the transmission protocol of Mode 2 and the baud rate generation method of Mode 1.

6.1.2 UART1 Operating Mode

Table 6-2: List of UART1 Operating Mode

SM	Mode	Description	Baud Rate
0	A	9-bit UART	Configurable
1	B	8-bit UART	Configurable

Mode A and Mode B of UART1 refer to Mode 3 and Mode 1 of UART0 respectively.

6.1.3 Multi-machine Communication

Mode 2 and Mode 3 of UART0, as well as Mode A of UART1, support multi-machine communication. In a multi-machine communication system, when the master intends to send a data block to one of multiple slaves, it first transmits an address byte to address the target slave. The address byte and the data byte can be distinguished by the 9th data bit, which is 1 for the address byte and 0 for the data byte. The receiver determines whether to receive data based on the information of the 9th bit. The multi-machine communication process is as follows:

- Master transmitting process:

  1. Set to the 9-bit mode, send the receiver address, and set TB8 = 1.
  2. Transmit the data according to the custom protocol, and set TB8 = 0.

- Master receiving process:

  1. Set SM2 = 0 (unconditionally receive all data).
  2. The master parses the data according to the custom protocol.

- Slave receiving process:

1. Set SM2 = 1 for the slave to be in the state of only receiving address frames, at this time only the address data with the 9th bit being 1 will be received.

2. When the data is received, the software determines whether it matches the serial port address configured for the local machine.

3. After all slaves receive the address frame, each compares the received address with its own address.

   - If there is a match (indicating it is the target slave), set SM2 = 0, prepare to receive the data frame that the master is about to send, and set SM2 = 1 again after receiving.

   - If there is no match, keep SM2 = 1, and ignore all subsequent data frames without generating interrupt requests until an address frame is received again for comparison and confirmation.

6.1.4 Baud Rate Error

When SYSCLK is 16 MHz, the configuration values of common baud rates SxREL and the actual errors are shown in the following table:

Table 6-3: Table of Baud Rate Error

Target Baud Rate	SxREL	Actual Baud Rate	Error
115200	1015	111111	3.5%
57600	1007	58824	-2.1%
38400	998	38462	-0.2%
19200	972	19231	-0.2%
9600	920	9615	-0.2%
4800	816	4808	-0.16%
2400	607	2398	0.08%

Note: The baud rate error data at 4 MHz is the same as that at 16 MHz.

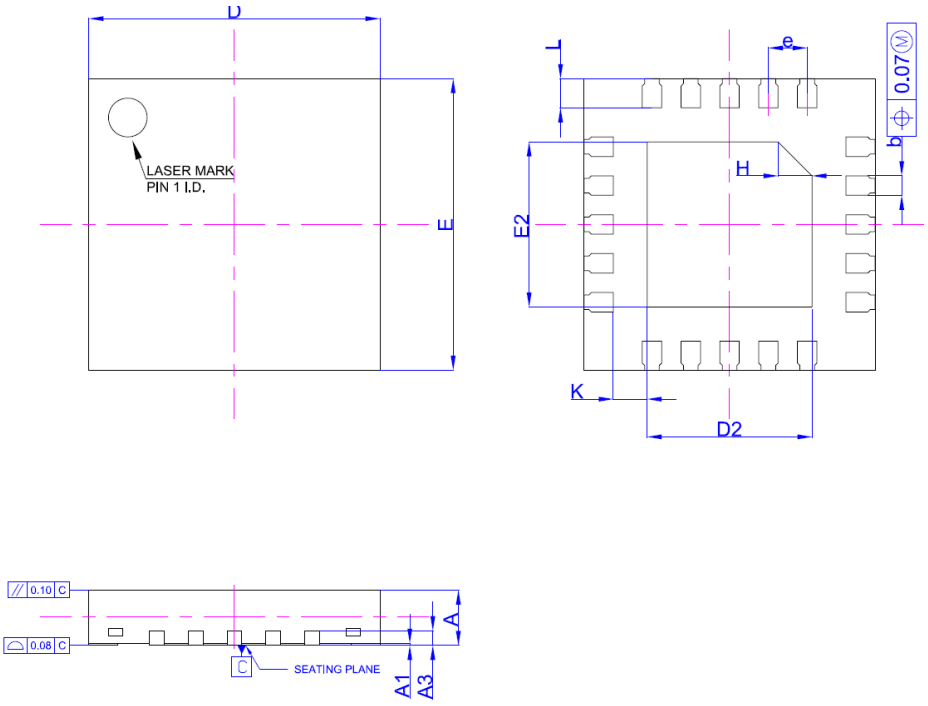
6.2 UART2/3

6.2.1 Main Features

- Providing standard asynchronous communication bits (start bit, parity bit, stop bit):
  - Generating a start bit
  - Generating a parity bit (odd or even), or no parity bit
  - Generating a stop bit
  - Bytes transmitted sequentially from LSB to MSB
- 8-bit 4-level RX FIFO
- Programmable baud rate (adjustable according to parameter F/D)
- Supporting data communication and error handling interrupts:
  - Status bit can be accessed by either polling or interrupt
  - Flags of FIFO non-empty, half-full, full, overflow
  - Parity error flag
- Validity check of start bit
- 2 * 8-bit baud rate parameter registers
- Supporting transfer at common baud rates such as 9,600 bps, 19,200 bps and 115,200 bps

7 Package Outline

7.1 QFN20 (3 * 3 mm)

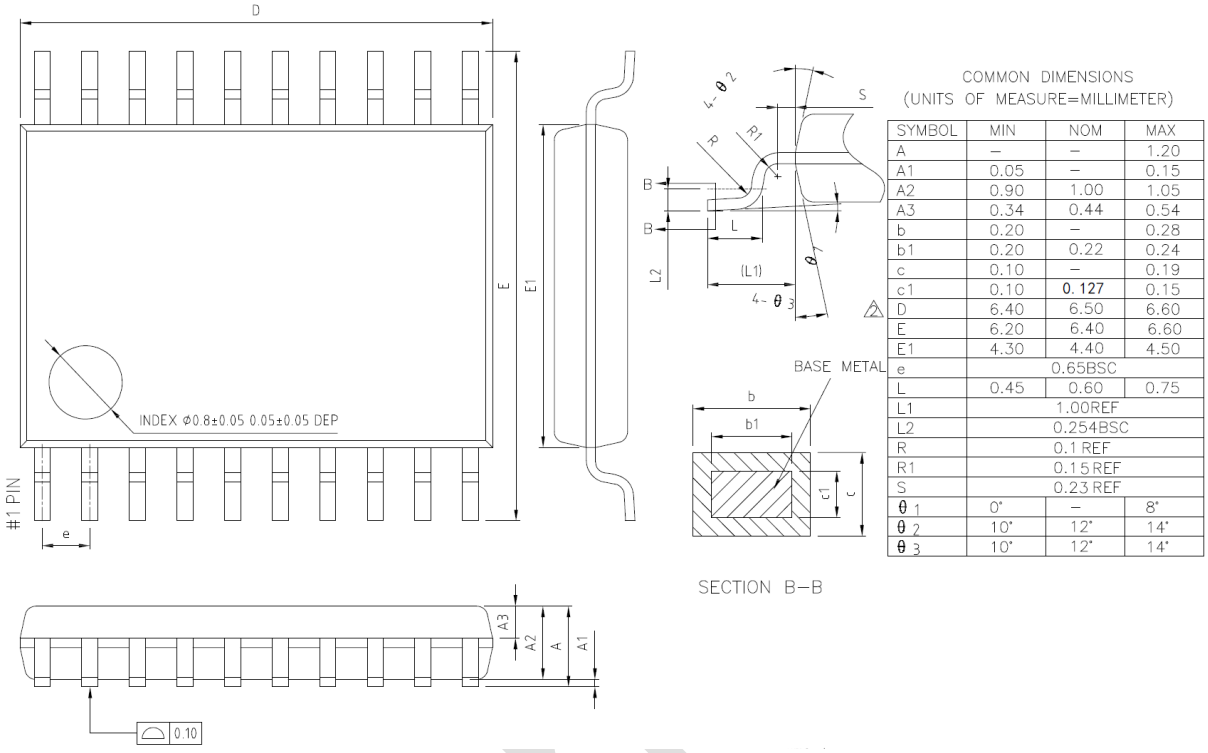


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3		0.152REF	
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.60	1.70	1.80
E2	1.60	1.70	1.80
b	0.15	0.20	0.25
L	0.225	0.30	0.375
e		0.40BSC	
H		0.35REF	
K		0.35REF	

Figure 7-1: QFN20 Package Outline

7.2 TSSOP20 (6.5 * 4.4 mm)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.127	0.15
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.254BSC		
R	0.1 REF		
R1	0.15 REF		
S	0.23 REF		
θ1	0°	–	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

Figure 7-2: TSSOP20 Package Outline

8 Revision History

Version	Date	Modifications
V1.0	Apr-10-2025	Initial release.
V1.0.1	May-12-2025	Added *Figure 4.3: Power Supply Scheme Diagram*.
V1.0.2	Jan-26-2026	1. Updated AIN pin naming. 2. Updated the junction temperature. 3. Updated package outline drawings.

9 Contact Us

Company: Unicmicro (Guangzhou) Co., Ltd.
Address:
Guangzhou: 12/F, Building B2, Grandtek IC Center, No. 18 Science Avenue, Huangpu District, Guangzhou, Guangdong
Postcode: 510700
TEL: +86-020-31600229

Shanghai: No. 1501, Building 2, 1077 ZuChongZhi Road, Zhangjiang High-Tech Park, Pudong District, Shanghai
Postcode: 201210
TEL: +86-021-50307225

Email: sales@unicmicro.com
Website: www.unicmicro.com