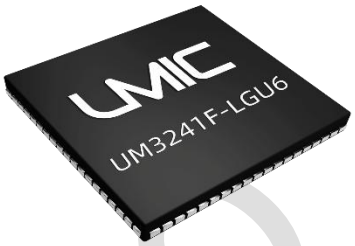
UNICMICRO 广芯微电子

UM3241F-LGU6

Low-power 32-bit MCU: ARM®Cortex®-M4 (FPU + DSP), 1 MB Flash, 160 KB + 32 KB + 4 KB SRAM, USB FS, Gigabit Ethernet, Encryption/Decryption Engines, 19 Timers, RTC, 2 x ADCs, 2 x DACs, Rich Communication and Camera Interfaces

Product Features

- **Low power management system**
  - 2 µA @ 3.0 V Standby mode, RTC running
  - 99 µA/MHz @ 3.0V @ 288 MHz Run mode
  - Integrated RTC, LPTIM, IWDT and LPUART
  - Low power modes: Sleep, Stop, Standby and DeepStandby
  - VBAT supply for RTC and 20 x 32-bit backup registers + optional 4 KB backup SRAM
- **Processor**
  - 32-bit ARM Cortex-M4
  - Integrated single-precision floating-point unit (FPU)
  - Integrated hardware DSP instruction unit
  - Memory protection unit (MPU)
  - Three-stage pipeline, with a maximum system clock frequency of 288 MHz
  - Single-cycle hardware multiplier
  - Integrated hardware divider
  - CPU performance reaches 360 DMIPS (1.25 DMIPS/MHz, 288 MHz)
  - CoreMark score as high as 992 (3.445 CoreMark/MHz, 288 MHz)
  - 4 KB instruction cache and 256-byte data cache, allowing 0-wait-state execution from Flash memory
- **Memory**
  - 160 KB SRAM (128 KB + 32 KB)
  - 32 KB Streaming SRAM
  - 4 KB Retention SRAM
  - 1MB Flash
- **GPIO**
  - Up to 67 I/O ports with interrupt capability
  - Multiple I/Os with 5 V tolerance



QFN76 (9 * 9 mm)

- **Reset and power management**
  - Power-on reset (POR) / Power-down reset (PDR) / Low-voltage detection (LVD) / Brown-out reset (BOR)
- **Clock**
  - Crystal oscillator from 1 MHz to 48 MHz
  - Internal 48 MHz RC oscillator
  - 32.768 kHz crystal oscillator with calibration function
  - Internal low-frequency 32 kHz RC oscillator
  - 2 x PLLs (supporting integer, fractional and spread spectrum functions), one of which is audio PLL
- **Communication interfaces**
  - Up to 6 UART interfaces (supporting 7/8/9 data bits, up to 10.5 Mbps), supporting IrDA control
  - Up to 2 USART interfaces, supporting UART/SPI/IrDA/LIN control
  - 1 x LPUART
  - 3 x I2C interfaces (up to 1 Mbps), supporting SMBus
  - 2 x I2S interfaces (supporting I2S/PCM formats)
  - Up to 4 general-purpose SPIs (up to 60 MHz)
  - Up to 36 PWM outputs (with 6 pairs of dead-time complementary outputs)

- 2 x CAN industrial buses, supporting CAN2.0B (up to 1 Mbps)
- One SDIO/SD/eMMC interface operating at 48 MHz, equipped with an independent dedicated DMA controller

- **Analog peripherals**
  - 2 × 12-bit ADCs, up to 5.25 Msps, 14 single-ended/differential channels
  - 2 × 12-bit DACs, 1 Msps, buffered outputs
  - 2 × operational amplifiers (OPAs) supporting single-ended PGA and comparator functions
  - Up to 3 analog comparators (ACMP)
  - Built-in temperature sensor (TS)

- **Timer**
  - 2 × 32-bit high-performance timers (eQCT™: TIM1/TIM8), each supporting 4 input captures, 3 pairs + 1 PWM output, 3 pairs of dead-time complementary outputs, and break function; supporting PWM precision up to 2 times the system clock frequency, with a maximum precision of 1.736 ns (576 MHz); supporting incremental quadrature encoder and Hall sensor.
  - 10 x 32-bit general-purpose timers (TIM2/TIM3/TIM4/TIM5/TIM9/TIM10/TIM11/TIM12/TIM13/TIM14), each supporting 4 input captures and 4 PWM outputs; supporting PWM precision up to 2 times the system clock frequency, with a maximum precision of 1.736 ns (576 MHz); supporting incremental quadrature encoder and Hall sensor.
  - 2 x 32-bit basic timers (TIM6/TIM7), able to trigger D/A conversion output
  - 2 x 16-bit low-power timers (LPTIM1/LPTIM2), each supporting 1 PWM output
  - 1 x low-power IWDT, resettable/interruptible
  - 1 x window watchdog timer (WWDT)
  - 1 x 24-bit SysTick timer

- **Real-time clock (RTC)**
  - Hardware perpetual calendar (with seconds, minutes, hours, weekday, date, month and year displayed in BCD format), with calibration supported

- **High-speed interfaces**
  - One Ethernet controller with DMA, supporting 10M/100M/1000M Ethernet (RGMII/RMII/MII interfaces)
  - One USB interface, supporting full-speed USB FS device interface (with integrated PHY)

- **Camera and display interfaces**
  - 8-bit to 14-bit DCMI with a data transfer rate up to 54 MB/s

- **Hardware acceleration co-processor**
  - Cordic accelerator (sin, cos, arctan, square root, multiplication, division, etc.)

- **Hardware encryption/decryption engine**
  - Hardware encryption/decryption: for AES (128/256) and SHA256
  - Random number generator
  - CRC calculation unit

- **Security**
  - Anti-copy board to prevent programs in Flash from being pirated
  - Hardware acceleration for data verification algorithms: CRC16-CCITT/CRC32
  - 128-bit UUID
- **Electrical parameters**
  - Operating voltage: 1.8 ~ 3.6 V
  - Operating temperature: -40 ~ 105℃

- **Moisture sensitivity level:** MSL-3
- **Development support**
  - Built-in Bootloader: supporting USB/UART download, and application updates via ISP and IAP
  - JTAG to SWD mode for online debugging and downloading
  - Complete SDK and EVB HDK
- **Ordering information**

Type	Part No.
1MB Flash	UM3241F-LGU6 (QFN76, 9 * 9 mm)

Contents

1 Product Introduction

The UM3241F-LGU6 chip is general-purpose microprocessors with high performance and low power consumption, based on the ARM® Cortex® -M4 core. The M4 core implements a full set of DSP (digital signal processing) instructions and features a floating-point unit (FPU) and a memory protection unit (MPU). The typical system clock frequency is 204 MHz (288 MHz @ boost mode). The built-in FLASH has a maximum capacity of 1 MB, while the SRAM has a maximum capacity of 160 KB, with 32 KB dedicated to DMA SRAM. They are available at a wide supply voltage of 1.8 V to 3.6 V and in the industrial temperature range from -40℃ to 105℃.

The UM3241F-LGU6 chip feature a rich set of peripherals, including:

- 1 x USB FS device interface
- 1 x SDIO/SD/eMMC interface
- 1 x 10/100M/1000M Ethernet interface
- 2 x 12-bit high-speed ADCs
- 2 x 12-bit DACs
- Built-in temperature sensor
- 3 x comparators
- 2 x operational amplifiers
- 2 x USARTs
- 6 x UARTs
- 4 x SPIs
- 3 x I2C interfaces

- 2 x I2S interfaces
- 2 x watchdog timers
- 2 x CAN bus interfaces
- 1 x QSPI
- 14 x counters/timers (including advanced controllers and general-purpose timers)
- 1 x low-power UART (LPUART)
- 2 x low-power timers (LPTIMx)
- 1 x 32-bit RTC clock and counter
- Up to 51 channels of general-purpose input/output (GPIO) ports
- Digital camera interface (DCMI)
- Integrated hardware CORDIC module (supporting sin, cos, arctan, square root, multiplication, and division)
- Built-in encryption/decryption engine (including AES, SHA, etc.)
- 1 x random number generator (RNG) that can generate random keys

Applications:

- Motor
- IoT, etc.

1.1 Functional Block Diagram

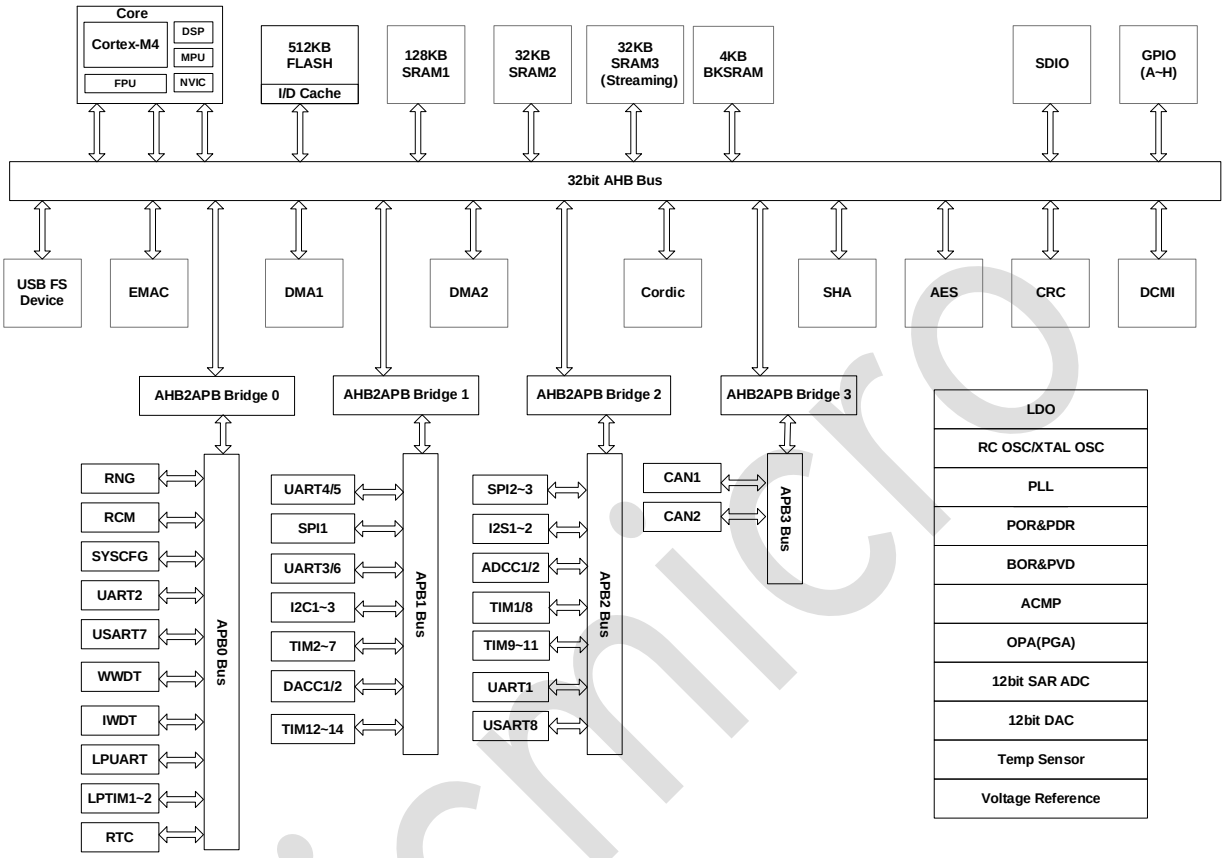


Figure 1-1: Functional Block Diagram

1.2 Configuration Table

Table 1-1: Configuration Table

Part No.		**UM3241F-LGU6**
Flash (KB)		512 + 512
SRAM (KB)	System	160 (128 + 32)
	Backup	4
DMA SRAM (KB)		32
Timer	General-purpose timer	10 (32 bits)
	Advanced control timer	2 (32 bits)
	Basic timer	2 (32 bits)
	SysTick	Yes
	IWDT	Yes
	WWDT	Yes
	LPTIM	2
	PWM channels	36
Communication interfaces	SPI	4
	I2S	2
	I2C	3
	USART	2
	UART	6
	LPUART	1
	CAN (2.0 B)	2
	USB FS device	1
	SDIO	1
Ethernet		GbE/FE
RTC		1
DCMI		1
GPIO		67
Analog	12-bit ADC Channels	2 14
	12-bit DAC Channels	2 2
	Internal voltage reference	Yes

Part No.		**UM3241F-LGU6**
	OPA (PGA)	2
	ACMP	3
	TS	Yes
Cordic		1
Hardware encryption/ decryption engine	CRC	Yes
	AES (256)	Yes
	SHA (256)	Yes
	RNG	Yes
Maximum CPU frequency		288 MHz
Operating voltage		1.8 ~ 3.6 V
Operating temperature		Ambient temperature: -40 ~ +85℃ / -40 ~ +105℃
		Junction temperature: -40 ~ +125℃
Package		QFN76 (9 * 9 mm)

2 Functional Overview

2.1 Core

The ARM Cortex™-M4F processor, the latest generation of embedded processors, is developed based on the Cortex™-M3 core, with strengthened computational capabilities, newly-added FPU, DSP and parallel computing instructions, delivering superior performance of 1.25 DMIPS/MHz. The combination of its efficient signal processing capabilities with the low power consumption, low cost, and ease of use of the Cortex-M series processors makes it ideal for applications requiring a mix of control and signal processing capabilities that are easy to use.

The ARM Cortex™-M4F is a 32-bit RISC processor with outstanding code efficiency.

2.2 Hardware Memory Accelerator

The memory accelerator optimized for the industrial-standard ARM Cortex™-M4F is provided with a 4KB instruction cache and a 256-byte data cache. It balances the inherent performance advantage of the ARM® Cortex™-M4F over the traditional Flash memory technologies, which requires the processor to wait for the Flash memory at higher operating frequencies. Based on Core-Mark benchmark, the performance achieved thanks to this accelerator is equivalent to 0-wait-state program execution from Flash memory at a CPU frequency of up to 288 MHz.

2.3 Memory

The chip integrates embedded Flash and embedded SRAM.

2.3.1 Embedded Flash

The chip integrates a 1 MB Flash for storing programs and data.

2.3.2 Embedded SRAM

Main features:

- Up to 160KB of system SRAM (128KB SRAM1 + 32KB SRAM2), including 128KB of SRAM1, which can be accessed by CPU with 0 wait cycle
- 4KB of backup SRAM
- 32KB of Streaming SRAM (SRAM3), supporting write operations by both CPU and DMA while read operation only by DMA and single-address read access by CPU

2.4 Nested Vectored Interrupt Controller (NVIC)

The nested vectored interrupt controller is able to handle multiple maskable interrupt channels (excluding the 16 Cortex™-M4F interrupt lines) and 16 priority levels.

- Tightly coupled NVIC gives low-latency interrupt processing
- Interrupt vector entry address goes directly into the core
- Tightly coupled NVIC interface
- Allowing early processing of interrupts
- Handling of late-arriving higher-priority interrupts
- Supporting interrupt tail chaining
- Automatic saving of processor state
- Automatic restoration upon interrupt return, with no additional instruction overhead

This module provides flexible interrupt management with minimal interrupt latency.

2.5 Clock Architecture

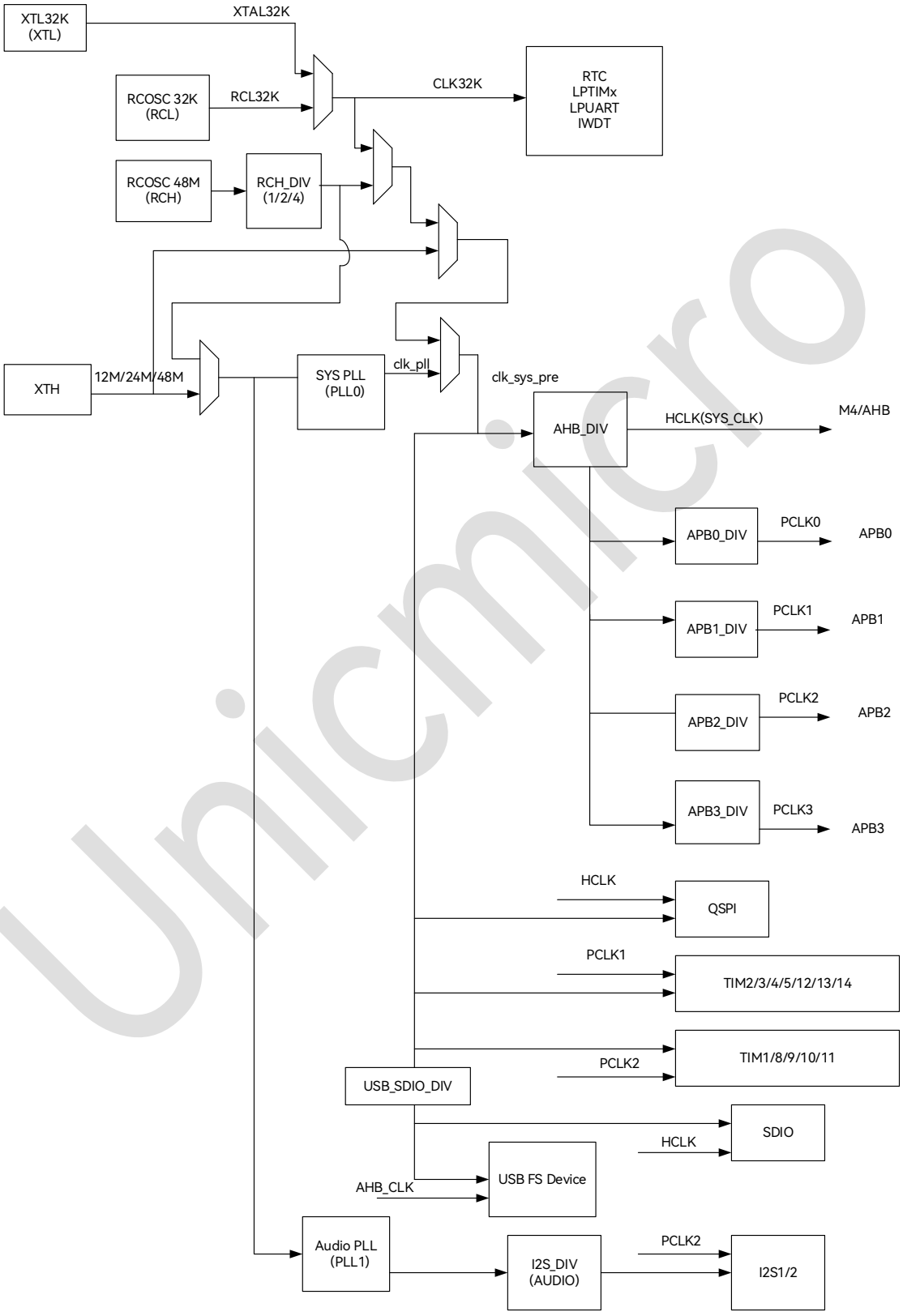


Figure 2-1: Clock Architecture Diagram

Four different sources can be used to drive the system clock:

- High-precision internal RCH of 48 MHz
- Internal RCL of 32 kHz
- External crystal XTL of 32.768 kHz
- External crystal XTH

There are two internal PLLs for system, audio and USB clocks.

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It features a 48 MHz internal RC oscillator (RCH), an external high-speed crystal oscillator (XTH), a 32 kHz internal RC oscillator (RCL), an external low-speed crystal oscillator (XTL), two PLLs, an XTH monitor, clock prescaler, clock multiplexer and clock gating circuitry.

AHB, APB and Cortex™-M4 are derived from the system clock (SYS_CLK), and the clock source of SYS_CLK can be XTH, RCH, PLL, or RCL/XTL with a low frequency of 32 kHz. The independent watchdog is clocked from a low-frequency RCL or XTL, and the RTC is clocked from RCL or XTL.

2.6 Reset

The chip reset modes are shown in the following table:

Table 2-1: Reset Mode

Reset Mode	Trigger Condition
Power-on and power-down reset (POR & PDR)	Power-on/power-down of V_{DDH} (1.8–3.6 V) and power-on of internal core voltage
RESETN pin reset	Low-level input on the external RESETN pin
Brownout reset (BOR)	V_{DDH} drops below the V_{BOR} threshold
Low voltage detection reset (LVD)	V_{DDH} drops below the V_{LVD} threshold
Window watchdog timer reset (WWDT)	-
Independent watchdog timer reset (IWDT)	-

Reset Mode	Trigger Condition
Power-down wakeup reset	Reset triggered by setting the power-down mode, with the core waking up from the reset state after a power-down wakeup event
Software reset	-
External high-speed oscillator failure reset	Reset triggered when the external high-speed oscillator stops abnormally

2.7 Power Management Unit (PMU)

The chip supports single power supply and VBAT backup power supply. It requires an external operating supply voltage between 1.8 V and 3.6 V, and a digital circuit operating voltage generated by the built-in LDO.

VDDH: 1.8 ~ 3.6 V, the VDDH pin supplies power to the I/O, the internal regulator and some analog IPs.

VDDA: 1.8 ~ 3.6 V, the VDDA pin supplies power to analog IPs such as ADC/DAC.

VBAT: 1.8 ~ 3.6 V, the VBAT pin supplies power to always-on modules such as BKSRAM and RTC in Standby mode.

It also supports multiple low-power modes: Sleep mode, Stop mode, Standby mode, and DeepStandby mode.

Table 2-2: Low-power Modes Summary

Power Mode	Descriptions	Entry Condition	Wakeup Source
Run mode	All supplies are powered on, and the high-speed clock remains active.	-	-

Power Mode	Descriptions	Entry Condition	Wakeup Source
Sleep mode	All supplies are powered on, with the M4 core high-speed clock off and other peripherals on.	1. PMU_STANDBY_EN = 0, PMU_MODE[1:0] = 00, PMU_BKSRAMOFF = 0 2. EFC_Sys_Mode = 0 3. WFI/WFE	1. Wake-up by any GPIO interrupt 2. Wake-up by any peripheral interrupt 3. Wake-up by reset (RESETN, IWDT reset)
Stop mode	All supplies are powered on, with the high-speed clock off and the 32 kHz low-speed clock on.	1. PMU_STANDBY_EN = 0, PMU_MODE[1:0] = 01, PMU_BKSRAMOFF = 0 2. EFC_Sys_Mode = 0 3. Set SLEEPDEEP = 1 for M4 core. 4. WFI/WFE	1. Wake-up by any GPIO interrupt 2. Wake-up by RTC alarm interrupt, RTC timestamp and tamper interrupts 3. Wake-up by IWDT reset or interrupt 4. Wake-up by external LPUART 5. Wake-up by LPTIM1–2 timing
Standby0 mode	The CORE domain is powered off, the BBU domain is kept on, and the 32 kHz low-speed clock remains active. BKSRAM/IWDT/ LPTIM/LPUART are powered on.	1. PMU_STANDBY_EN = 1, PMU_MODE[1:0] = 10, PMU_BKSRAMOFF = 0 2. EFC_Sys_Mode = 1 3. Set SLEEPDEEP = 1 for M4 core. 4. WFI/WFE	1. Wake-up by external pins PA0, PA2, PC0, PC2 and PC3 2. Wake-up by RTC alarm interrupt, RTC timestamp and tamper interrupts 3. Wake-up by LPTIM1–2 timing 4. Wake-up by LPUART (only PC2) 5. Wake-up by IWDT reset or interrupt 6. Wake-up by reset (RESETN)

Power Mode	Descriptions	Entry Condition	Wakeup Source
Standby1 mode	The CORE domain is powered off, the BBU domain is kept on, and the 32 kHz low-speed clock remains active. BKSRAM/IWDT/ LPTIM/LPUART are powered off.	1. PMU_STANDBY_EN = 1, PMU_MODE[1:0] = 10, PMU_BKSRAMOFF = 1 2. EFC_Sys_Mode = 1 3. Set SLEEPDEEP = 1 for M4 core. 4. WFI/WFE	1. Wake-up by external pins of PA0, PA2, PC0, PC2, PC3 and PC13 2. Wake-up by RTC alarm interrupt, RTC timestamp and tamper interrupts 3. Wake-up by reset (RESETN)
DeepStandby mode 0	The CORE domain is powered off, the BBU domain is kept on, and the 32 kHz low-speed clock is inactive. BKSRAM/IWDT/ LPTIM/LPUART are powered on.	1. PMU_STANDBY_EN = 1, PMU_MODE[1:0] = 11, PMU_BKSRAMOFF = 0 2. EFC_Sys_Mode = 1 3. Set SLEEPDEEP = 1 for M4 core. 4. WFI/WFE	1. Wake-up by external pins of PA0, PA2, PC0, PC2, PC3 and PC13 2. Wake-up by reset (RESETN)
DeepStandby mode 1	The CORE domain is powered off, the BBU domain is kept on, and the 32 kHz low-speed clock is inactive. BKSRAM/IWDT/LPTIM/LPUART are powered off.	1. PMU_STANDBY_EN = 1, PMU_MODE[1:0] = 11, PMU_BKSRAMOFF = 1 2. EFC_Sys_Mode = 1 3. Set SLEEPDEEP = 1 for M4 core. 4. WFI/WFE	1. Wake-up by external pins of PA0, PA2, PC0, PC2, PC3 and PC13 2. Wake-up by reset (RESETN)
Power-off mode	All supplies are powered off.	Powering off external VDDH & VBAT	Power on

Notes:

- The BBU domain includes RTC, backup register and PMU logic.
- Sleep mode and stop mode support IO retention.
- Standby mode and DeepStandby mode do not support IO retention, except for the IOs used for external wake-up, other IOs are in high-impedance state. After wake-up, the IO pins are in the power-on reset state.

2.8 Boot Mode

The system executes from address 0x0000_0000 upon power-on of the chip.

Table 2-3: Boot Mode

BOOT1 (PB2)	BOOT0	Boot
0	0	Boot from main Flash
1	0	Reserved
0	1	Boot from system memory
1	1	Boot from SRAM (reserved)

Note: Operating the BOOT_SOURCE address in the user area can directly boot from main Flash, which speeds up the chip power-on time.

2.9 Direct Memory Access Controller (DMA)

The DMA is used to provide high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions, which keeps the CPU resources free for other operations, thus improving the system efficiency.

The chip embeds two DMA controllers (DMA1 /DMA2), supporting a total of 16 channels.

Main features:

- Can control data transfer among multiple modules
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral data transfers
- Each controller is provided with 8 DMA channels.
- Configurable bit width and block length of data transfer
- Each channel with 4 x 32-bit FIFOs
- Block length up to 4095
- Supporting fixed and incremental source address transfers
- Supporting fixed and incremental destination address transfers

2.10 Universal Asynchronous Receiver Transmitter (UART)

UART is a widely used serial communication interface that supports full-duplex communication. The UART converts parallel data from memory or a processor into serial data for transmission to an external UART receiver, or it converts serial data received from an external UART device into parallel data for the processor. UART supports serial communication with external interface devices.

Main features:

- 16-byte hardware FIFO
- Baud rate supports both integer and fractional division
- CTS/RTS flow control

- Error start bit detection
- Frame interrupt detection
- Circuit-break detection
- Setting of data bit width (5–9 bits) and number of stop bits (1 bit, 1.5 bits and 2 bits)
- Fixed parity, even/odd parity or no parity for data
- IrDA 1.0 protocol with baud rate ranging from 9.6 k to 115.2 k
- DMA operation

2.11 Universal Synchronous / Asynchronous Receiver Transmitter (USART)

USART provides a complete full-duplex universal synchronous / asynchronous serial link. To ensure the highest standard, the data frame format can be programmed in a wide range (data length, parity, number of stop bits, etc.) This receiver implements detection of parity error, frame error and overflow error. Receiver timeout allows handling of frames with variable lengths, and transmitter time protection facilitates communication with slow remote devices. Multiprocessor communication can also be supported by address bit processing in reception and transmission.

Main features:

- Programmable baud rate generator
- 5-bit to 9-bit full-duplex synchronous or asynchronous serial communication
  - 1, 1.5 or 2 stop bits in asynchronous mode; or 1 or 2 stop bits in synchronous mode
  - Parity generation and error detection
  - Frame error detection and overflow error detection

- MSB first or LSB first for data transfer
- Optional open-circuit mark generation and detection
- Receiver sampling rate of 8 or 16 times the baud rate
- Optional hardware handshake RTS – CTS
- Receiver timeout and transmitter time protection
- Optional multipoint mode with address generation and detection

- IrDA modulation/demodulation
  - Communication rate up to 115.2 kbps
- SPI mode
  - Master or slave
  - Programmable serial clock phase and polarity
  - SPI serial clock (SCK) frequency up to 1/2 of the internal clock frequency
- LIN mode
  - Complying with LIN1.3 and LIN2.0 specifications
  - Master or slave
  - Handling frames of up to 256 data bytes
  - Response data length configurable or automatically defined by the identifier
  - Self-synchronization in slave node configuration
  - Automatic processing and verification of “Synch Break” and “Synch Field”
  - Detection of “Synch Break” even if it is partially overlapped with a data byte
  - Automatic identifier parity calculation, transmission and verification
  - Parity transmission and verification can be disabled

- Automatic checksum calculation, transmission and verification
- Checksum transmission and verification can be disabled
- Supporting both “Classic” and “Enhanced” checksum types
- Complete LIN error checking and reporting

- DMA operation

2.12 Low-power Universal Asynchronous Receiver Transmitter (LPUART)

LPUART is a low-power UART that supports data reception at a maximum baud rate of 9600 Hz when operating at 32 kHz clock.

Main features:

- Asynchronous data transmission and reception
- Standard UART frame format
  - 1 start bit
  - 7 or 8 data bits
  - Odd parity, even parity or no parity bit
  - 1 or 2 stop bits
- Operating with a 32768 Hz XTL clock or a 32 kHz RCL clock, supporting baud rates from 300 to 9600 Hz
- Programmable data polarity
- Interrupt flags

- Receive buffer full flag
- Receive buffer overflow flag
- Receive frame format error flag
- Receive parity bit error flag
- Start detection flag
- Data matching flag
- Transmission complete flag

- Wake-up in low-power mode
  - Wake-up on RXD falling edge interrupt
  - Wake-up on start bit detection
  - Wake-up on completion of receiving 1 byte
  - Wake-up on matching 1 byte of data

2.13 General-purpose Input/Output (GPIO)

Up to 51 GPIOs are available. Each port is controlled by an independent control register bit. They support edge-triggered interrupts and level-triggered interrupts to wake up the chip from various low-power modes to run mode. They are integrated with pull-up and pull-down resistors with Schmitt trigger input filtering function. The output drive capability is configurable, with a maximum current drive capability of 12 mA. The 51 GPIOs support external asynchronous interrupts, wherein, multiple GPIOs can support 5 V withstand voltage input.

2.14 Timer / Counter (TIMx)

2 x 32-bit high-performance timers (eQCT™: TIM1/ TIM8), each timer supports 4 input captures, 3 pairs + 1 PWM output, 3 pairs of dead-time complementary outputs, break function, PWM precision at twice the system clock frequency; and supports incremental quadrature encoder and Hall sensor.

10 x 32-bit general-purpose timers (TIM2/ TIM3/ TIM4 / TIM5/ TIM9/ TIM10/ TIM11/ TIM12/ TIM13 / TIM14): each timer supports 4 input captures and 4 PWM outputs, PWM precision at twice the system clock frequency; and supports incremental quadrature encoder and Hall sensor.

2 x 32-bit basic timers (TIM6/ TIM7): able to trigger DAC output.

The timer functions are compared as follows:

Table 2-4: Timer Function Comparison

Timer Type	Timer	Resolution	Type	Prescaler Factor	DMA Request Generation	Capture/ Compare Channels	Complementary Output
Advanced timer	TIM1 TIM8	32	Up, down, up/down	Any integer between 1 and 65536	Y	4	Y
General-purpose timer	TIM2 TIM3 TIM4 TIM5 TIM9 TIM10 TIM11 TIM12 TIM13 TIM14	32	Up, down, up/down	Any integer between 1 and 65536	Y	4	N

Timer Type	Timer	Resolution	Type	Prescaler Factor	DMA Request Generation	Capture/ Compare Channels	Complementary Output
Basic timer	TIM6 TIM7	32	Up	Any integer between 1 and 65536	Y	0	N
Low-power timer	LPTIM1 LPTIM2	16	Up	Any integer between 1 and 65536	N	1	N

2.15 Low-power Timer (LPTIM)

LPTIM is a 16-bit low-power timer/counter module running in always-on power domain. By selecting suitable clock source, LPTIM is able to keep running in various low-power modes with extremely low power consumption. LPTIM can be used as an external pulse counter in low-power mode even with no internal clock source. Also, in combination with an external input trigger signal, LPTIM is able to realize timeout wake-up from low-power modes.

Main features:

- 16-bit up counter
- 3-bit asynchronous prescaler with 8 possible dividing factors (1, 2, 4, 8, 16, 32, 64, 128)
- Selectable clock sources:
  - Internal clock sources: LSCLK (XTL or RCL), CLK1HZ, APB0 (PCLK0)
  - External clock source: LPTIMx_IN
- 16-bit compare register
- 16-bit target register
- Software/hardware trigger

- Configurable input polarity
- External pulse counting with no clock source
- Externally triggered timeout wake-up from low-power modes
- 16-bit PWM

2.16 Inter-integrated Circuit (I2C) Interface

The device embeds three I2Cs (I2C1/I2C2/I2C3), supporting master and slave modes.

Main features:

- Master receive/transmit, slave receive/transmit
- Up to 1 Mbps operating rate
- 7-bit and 10-bit addressing mode
- Interrupt polling
- RX FIFO and TX FIFO with a depth of 2 bytes each
- DMA acceleration

2.17 Real-time clock (RTC)

The RTC supports calendar with subsecond, seconds, minutes, hours, week day, date, month and year displayed in BCD (binary-coded decimal) format; and also supports an alarm, a periodic wake-up source, a tamper detector and an 80-byte backup register.

2.18 Inter-integrated Sound (I2S) Interface

The Inter-IC Sound Bus (I2S) is a standardized communication interface developed by Philips for use in many (super) large-scale IC-based systems, especially in many digital stereo audio systems.

Main features:

- Master and slave modes
- Simplex transmitting, simplex receiving, duplex transceiving
- Philips standard, left-justified and right-justified standards, PCM (with short and long frame) standard
- Configurable audio channel length: 16 or 32 bits
- Configurable audio data length: 8, 16, 24 or 32 bits
- For non-PCM standard, both stereo and mono audio data are available.
- The stereo audio data can be transmitted via left channel first or via right channel first.
- The mono audio data can be transmitted via left channel or right channel.
- For non-PCM standard, the polarity of WS is optional.
- For non-PCM standard, the moment of switching between SD and WS is optional on the rising or falling edge of SCK; while for PCM standard, it is fixed on the rising edge of SCK.
- Built-in 8-word TX FIFO and RX FIFO (1 word = 32 bits), each can store 16 pieces of 16-bit data or 8 pieces of 32-bit data.
- MCLK generated by PLL is required when audio block is defined as master at 256 times the audio sampling rate (Fs), which is typically 8/11.025/16/22.05/24/32/44.1/48/96/192 kHz.

- If interrupt is enabled, the following conditions will trigger an interrupt:
  - TX FIFO with enough space
  - RX FIFO with enough data
  - TX FIFO underrun
  - RX FIFO overflow
- DMA operation

2.19 Controller Area Network (CAN)

The CAN controller being compliant with CAN2.0A/B protocol can be used in the fields of automotive electronics and industrial control.

Main features:

- In compliant with CAN2.0A/B protocol
- Supporting CAN format
- Up to 8 bytes data frame
- Up to 1 Mbps in CAN2.0B
- 64-byte RX FIFO
- 16-byte TX FIFO
- Transfer stop available
- Readable error counter

2.20 Serial Peripheral Interface (SPI)

The synchronous serial interface supports both master and slave modes. It also supports DMA hardware data transfer.

SPI is widely used to provide an economical board-level interface between different devices such as EEPROM, FLASH, micro-controller, DAC, ADC, etc.

Main features:

- Configurable master or slave mode
- Supporting serial full duplex, half duplex, simplex transmitting and simplex receiving in both master and slave modes
- Configurable 16-bit SPI clock frequency control register: SCK frequency up to $f_{PCLK}/2$ in master mode while up to $f_{PCLK}/4$ in slave mode
- Configurable SCK polarity and phase
- Configurable SPI Motorola mode or TI mode
- Configurable data transmission or reception order of MSB first or LSB first
- Configurable character length from 4 to 32 bits, defaulting to 8 bits
- Supporting data concatenation to fully utilize FIFO space
- Featuring 8-level 32-bit wide TX FIFO and RX FIFO
- Programmable software- or hardware-controlled chip select
- DMA operation

2.21 Quad-SPI Controller (QSPI)

The QSPI is a specialized communication interface targeting single, dual or quad SPI Flash memories.

Main features:

- Memory-mapped direct-access mode for Flash data transfer and code execution from Flash memory
- Software-triggered indirect-access mode for low-latency and non-processor-intensive Flash data transfer
- DMA operation
- Software-accessible APB Flash control register set can execute any Flash command, including data transfers of up to 8 bytes per transaction
- Supporting XIP (Execute in Place), also known as continuous mode
- Supporting single-SPI, dual-SPI and quad-SPI modes
- Programmable device size
- Programmable write protection zones preventing system-initiated writes
- Programmable inter-transfer delays
- Allowing direct software access to underlying TX and RX FIFOs in traditional mode, bypassing higher-layer processes
- Supporting an independent asynchronous SPI communication reference clock
- Serial clock with configurable polarity

- Programmable baud rate generator supports generation of different device clocks
- With features for enhancing the capture mechanism of high-speed data reading
- Optional use of an adjusted clock to further enhance read data capture
- Programmable interrupt generation
- Supporting one external device

2.22 Independent Watchdog Timer (IWDT)

The watchdog timer can generate a non-maskable interrupt or reset when the counter reaches the given timeout value. It can be used to regain control when the system fails to respond as expected due to software errors or external device failures.

Main features:

- 32-bit downcounter with programmable load
- Independent watchdog timer enabled
- Interrupt generation logic with interrupt masking
- Software runaway protection lock register
- Software-initiated function: reset enable/disable setting in WDT control register
- Register configuration to pause timer counting when the CPU is suspended during debugging

2.23 System Window Watchdog (WWDT)

The system window watchdog is a watchdog running synchronously with CPU, aiming at monitoring the running status of CPU in real time, so that it can reset CPU in the case of abnormal operation to avoid unpredictable consequences.

To ensure synchronization and real-time performance, the WWDT operates using the PCLK clock, with an internal prescaler circuit to generate a synchronous counting enable signal.

Main features:

- In up-counting mode, the counter counts from 0 to the overflow time.
- The window period is defined as the period when the counter is greater than or equal to 50% of the overflow time.
- With early warning interrupt function, which triggers an interrupt at 75% of the overflow time.

2.24 Hardware Acceleration Co-processor (CORDIC)

The CORDIC provides hardware acceleration of certain mathematical functions such as $m \cdot \sin\theta$, $m \cdot \cos\theta$, $\mathrm{atan2(y,x)}$, $\sqrt{x^2+y^2}$, $y \cdot x$, $\mathrm{y/x}$, $\sinh w$, $\cosh w$, $\tanh^{-1}(y/x)$, $\ln x$, $\sqrt{\mathrm{x}}$, etc.

Main features:

- 24-bit CORDIC rotation engine
- AHB interface supporting input and output of 16-bit and 32-bit data

2.25 Secure Digital Input and Output (SDIO)

As a data transfer interface, SDIO controller compliant with SD and eMMC standard protocols can be used as the master controller of SD card reader and eMMC card reader, and also supports secure digital I/O.

Main features:

- SD2.0 and eMMC4.4.1 protocols
- Built-in FIFO with a width of 32 bits and a depth of 16, can stop the clock at overrun and underrun
- CRC generation and verification
- Programmable baud rate Programmable baud rates, with a clock division ratio to meet the requirements for communication at various baud rates
- Clock control switching
- Card detection
- Card write protection
- Supporting SDIO interrupts in 1-bit, 4-bit, and 8-bit modes
- Block size ranging from 1 to 65536 bytes
- Equipped with an independent dedicated DMA controller, supports DMA transfer

2.26 Digital Camera Interface (DCMI)

The DCMI can receive 8/10/12/14-bit data streams from the camera and supports multiple formats and JPEG transfers.

Main features:

- 8/10/12/14-bit DVP interface
- Hardware/embedded code synchronization
- Continuous/single frame mode
- Window cropping function
- Built-in DMA data transfer

2.27 Ethernet Media Access Controller (EMAC)

The EMAC can receive and transmit Ethernet data, complying with the IEEE 802.3-2002 standard.

Main features:

- Supporting external PHY interface for data transfer rates of 10M/100M/1000M bit/s
- Supporting MII, RMII, and RGMII interfaces
- Full-duplex and half-duplex operation modes
- Configuring and managing PHY devices using MDIO interface
- Supports Ethernet timestamping (IEEE 1588-2002), providing a 64-bit timestamp for each frame in the transmit or receive state
- Preamble and start -of-frame delimiter (SFD) being inserted in the transmit path and removed in the receive path
- Validity detection of frame length supported for discarding ultra-long and ultra-short frames

- CRC check on incoming frames for discarding frames with errors
- CRC check on outgoing frames
- Short frame padding
- Statistical counting of received and transmitted frames
- Filtering of broadcast, multicast and unicast frames
- Configurable rate-limiting processing for control messages, IP messages, and broadcast or multicast messages
- Packet filtering
- Enqueuing interrupt and timeout interrupt
- Receive and transmit packets buffering
- Supporting energy-efficient Ethernet (EEE)
- Two independent 2K-byte FIFOs for transmission and reception respectively

2.28 Random Number Generator (RNG)

The RNG is capable of delivering true random numbers. RNG is capable of delivering true random numbers from random seeds.

2.29 Advanced Encryption and Decryption Algorithm Accelerator (AES)

The AES module encrypts or decrypts data using AES-128 or AES-256 algorithm defined in Federal information processing standards (FIPS) publication 197.

Main features:

- Cipher key lengths of 128 or 256 bits
- Supporting multiple chaining modes: CBC, ECB, ETR, CCM, CMAC and GCM
- Supporting encryption and decryption
- All data is in big-endian order according to AES regulations.
- Separate interfaces for key and message: low-capacity interface for key, and FIFO interacting with the interface for data input and output
- Using DMA for data input and output
- Instant key expansion available, no additional storage space required
- For a message, only packet-based encryption and decryption are supported, while message switching is not supported.
- Supporting three-key mode

2.30 Secure Hash Algorithm Accelerator (SHA)

The SHA module can implement the SHA-256 algorithm defined in FIPS publication 180-4.

Main features:

- 256-bit ICV length
- Information in external storage shall be in little-endian order with double words aligned
- Using a 32 x 32-bit input data FIFO
- Using DMA for data input

2.31 Universal Serial Bus Full-speed Device Interface (USB)

The USB device controller is a device interface compatible with the USB 2.0 full-speed protocol. It is used in conjunction with the USB PHY to support communication between the chip and the USB HOST.

Main features:

- Compatible with USB1.1 and USB2.0 full-speed protocols
- 4 general-purpose bidirectional transfer endpoints (EP1, EP2, EP3, EP4)
- Endpoints with a maximum packet length of 64 bytes, and supporting both memory and FIFO accesses
- FIFO mode supporting 32-bit access
- Memory access mode: 8-bit, 16-bit, 32-bit
- Suspend, resume and remote wake-up functions
- Hardware toggle comparison and software control functions
- Interrupt generation for data transfer on each endpoint
- Interrupt enabled for bus reset, suspend and resume
- Optional CRC error reply with NAK
- Automatic reply with NAK for data packets exceeding the maximum packet length (64 bytes)
- USB device reply with NAK for the next IN operation if the host does not reply with ACK for the IN operation
- Supporting detection of lost EOP in token packets and data packets, and optional automatic NAK response for lost EOP

2.32 Analog-to-digital Converter (ADC)

The device embeds two 12-bit SAR ADCs with the sampling rate of 5.25 Msps, supporting single-ended and differential inputs, and capable of measuring 14 external channels and 1 internal channel.

Main features:

- 12-bit successive approximation ADC
- ADC supply: 1.8–3.6 V; ADC input range: $V_{REF-} \leq V_{IN} \leq V_{REF+}$
- V_{REF} reference uses V_{DDA}
- The two ADCs can be used in conjunction with the internal operational amplifier (OPA) to amplify the signal before sampling or as buffers.
- Trigger mode: triggered by software configuration register, or internal timer event (rising edge, falling edge or both edges), or GPIOA interrupt
- Conversion modes: single-shot mode, continuous mode, discontinuous mode, dual-ADC cooperative mode
- Regular and injection sequences: A regular group is composed of up to 16 channel conversions, and an injected group is composed of up to 4 channel conversions. Both groups consist of a sequence of conversions that can be done on any channel and in any order. The injection sequence has higher priority over the regular sequence.
- It is able to continuously handle multiple times (2, 4, 8, 16, 32, 64 or 128 times) sampling conversions on one or some channels and calculate the average.
- It is provided with an analog watchdog for monitoring the conversion result.

- Each channel has an independent data register, which can be uniformly set to clear data automatically after reading.
- Each of the ADCs is provided with a 32-level deep and 16-bit wide RX FIFO for storing the conversion results of the regular and injection conversions.
- DMA mode supported

2.33 Digital-to-analog Converter (DAC)

Two independent DAC modules can be used to convert 12-bit digital signals into analog voltage signal outputs.

Main features:

- 8-bit or 12-bit digital input
- Simultaneous update of conversion data for two converters
- Generation of triangular waves and noise waves
- DMA operation
- External trigger to update conversion data

2.34 Operational Amplifier (OPA)

Main features:

- Supporting OPA function
- Supporting single-ended PGA (programmable gain amplifier) function with internal feedback resistors in 1/2/4/8x gain settings, and supporting PGA function with external

feedback resistors in 1/2/4/8/16/32/64x gain settings

- Can be used as an analog comparator
- Can be used as a buffer to cooperate with ADC

2.35 Analog Comparator (ACMP)

The ACMP module is used to compare the magnitudes of two input analog voltages and output a high or low level based on the comparison result. When the voltage at the “INP” input pin is higher than that at the “INM” input pin, the comparator outputs a high level; when the voltage at the “INP” input pin is lower than that at the “INM” input pin, the comparator outputs a low level.

Main features:

- The analog comparator output can generate an interrupt.

2.36 Temperature Sensor (TS)

The temperature sensor (TS) generates a voltage that varies linearly with temperature. It is internally connected to the ADC input channel which is used to convert the sensor output voltage into a digital value.

2.37 Security System

2.37.1 UID

Each chip is shipped with a 16-byte unique device identifier, including wafer lot information, chip coordinate information, etc.

2.37.2 CRC16/32 Hardware Cyclic Redundancy Check Code

The CRC controller can perform cyclic redundancy calculations using various polynomials.

Main features:

- Supporting the following polynomials:
  - $x^{16} + x^{12} + x^5 + 1$
  - $x^{16} + x^{15} + x^2 + 1$
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + 1$
- Input data types: byte, half-word, word
- The input data can be reversed by bit, half-word, byte, initial value and result value.

2.38 Debugging and Programming System

The debugging and programming system features are as follows:

- **Embedded debugging system**

  The embedded debugging solution provides a full-featured real-time debugger with standard and mature debugging development software such as Keil/IAR, supporting 4 hardware breakpoints and multiple soft breakpoints.

- **Online programming mode**

  Online programming is supported, and several milliseconds after reset it is in ISP mode, followed by user mode.

- **High security**

  The encrypted embedded debugging solution provides a full-featured real-time debugger.

3 Pin Definition and Description

3.1 Pin Definition

The chip comes in a variety of packages. The pin functions are configured by the IO control register, and all pins except the power pin and the RESETN pin are configured with alternate functions. After system reset, the pin functions will be set to their default values.

Note: The final package may have minor differences in some pins.

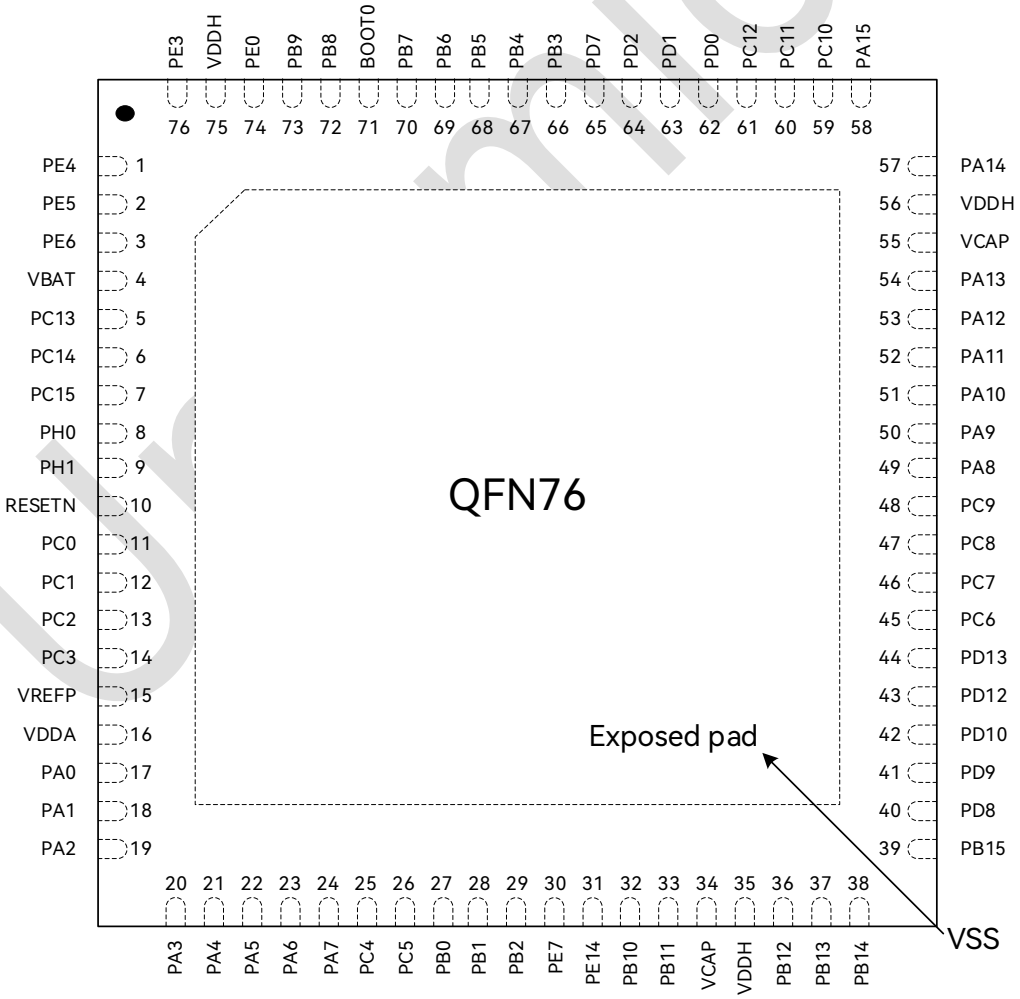


Figure 3-1: QFN76 (9 * 9 mm) Pinout Diagram

3.2 Pin Description

Table 3-1: Abbreviation Definition

Name	Abbreviation	Definition
Pin Name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name.	
Type	S	Power supply pin
	I	Input-only pin
	I/O	Input/output pin
I/O structure	FT	5 V tolerant I/O with fail-safe support
	TTa	3.3 V tolerant I/O with fail-safe support, directly connected to ADC, etc.
	B	Dedicated BOOT0 pin
	RST	Input reset pin with weak pull-up resistor
Alternate function	Function selected through GPIOx_AFR register	
Optional function	Function directly selected/enabled through peripheral registers	
Note	Unless otherwise specified in notes, all IOs are set to floating input (analog function, high-impedance state) during and after reset.	

Table 3-2: Pin Definition

Pin No.	Pin Name (After Reset)	Type	I/OStructure	Fail-safe Support	Optional Alternate Function		Note
					Alternate function	Optional function	
0	VSS(E-PAD)	-	-	-	-	-	-
1	PE4	I/O	FT	Yes	LPTIM1_OUT/ TIM9_CH4/ SPI4_NSS	-	-
2	PE5	I/O	FT	Yes	TIM9_CH1/ SPI4_MISO	-	-
3	PE6	I/O	FT	Yes	TIM9_CH2/ SPI4_MOSI	-	-
4	VBAT	S	-	-	-	-	Tie to ground unless VBAT and VDDH are supplied by two independent power sources (e.g., VBAT tied to a battery)
5	PC13-TAMPER-RTC	I/O	TTa	Yes	-	TAMPER-RTC/ WKUP	Supports only tamper and GPIO functions. When RESETN = 0, this pin features internal pull-down.
6	PC14-XTL_IN	I/O	TTa	Yes	-	XTL_IN	-
7	PC15-XTL_OUT	I/O	TTa	Yes	-	XTL_OUT	-
35/ 56/ 75	VDDH	S	-	-	-	-	-
8	PH0-XTH_IN	I/O	TTa	-	-	XTH_IN	-

Pin No.	Pin Name (After Reset)	Type	I/OStructure	Fail-safe Support	Optional Alternate Function		Note
					Alternate function	Optional function	
9	PH1-XTH_OUT	I/O	TTa	-	-	XTH_OUT	-
10	RESETN	I	RST	-	-	-	Default to pull-up
11	PC0	I/O	TTa	Yes	LPTIM1_IN/ TIM5_CH1/ USART7_CTS	ADC_IN10/ ACMP3_INM	-
12	PC1	I/O	TTa	Yes	LPTIM1_OUT/ TIM5_CH2/ USART7_RTS/ ETH_MDC/ EVENTOUT	ADC_IN11/ ACMP3_INP	-
13	PC2	I/O	TTa	Yes	LPUART_RX/ TIM5_CH3/ SPI2_MISO/ I2S1_EXTSD/ USART7_TX/ ETH_TXD2	ADC_IN12	-
14	PC3	I/O	TTa	Yes	LPTIM1_TRIG/ TIM5_CH4/ SPI2_MOSI/ I2S1_SD/ USART7_RX/ ETH_TX_CLK	ADC_IN13	-
15	VREFP	S	-	-	-	-	

Pin No.	Pin Name (After Reset)	Type	I/OStructure	Fail-safe Support	Optional Alternate Function		Note
					Alternate function	Optional function	
16	VDDA	S	-	-	-	-	-
17	PA0	I/O	TTa	Yes	TIM2_CH1_ETR/ TIM5_CH1/ TIM8_ETR/ UART2_CTS/ UART4_TX/ USART7_CTS/ ETH_CRS	ADC_IN0/ OPA1_VINP	-
18	PA1	I/O	TTa	Yes	TIM2_CH2/ TIM5_CH2/ UART2_RTS/ UART4_RX/ USART7_RTS/ ETH_RX_CLK/ ETH_REF_50M/ EVENTOUT	ADC_IN1/ OPA1_VINM	-
19	PA2	I/O	TTa	Yes	TIM2_CH3/ TIM5_CH3/ TIM9_CH1/ UART2_TX/ UART4_CTS/ USART7_TX/ ETH_MDIO	ADC_IN2	-

Pin No.	Pin Name (After Reset)	Type	I/OStructure	Fail-safe Support	Optional Alternate Function		Note
					Alternate function	Optional function	
20	PA3	I/O	TTa	Yes	TIM2_CH4/ TIM5_CH4/ TIM9_CH2/ UART2_RX/ UART4_RTS/ USART7_RX/ ETH_COL	ADC_IN3/ OPA1_VOUT	-
21	PA4	I/O	TTa	No	LPUART_TX/ TIM1_CH3/ SPI1_NSS/ SPI3_NSS/ I2S2_WS/ USART7_CK/ DCMI_HSYNC	DAC1_OUT	Note 2; cannot be used as an external ADC input channel. Pull-up disabled.
22	PA5	I/O	TTa	Yes	TIM2_CH1_ETR/ TIM1_CH4/ TIM8_CH1N/ SPI1_SCK/ TIM13_CH2	DAC2_OUT	Note 2; cannot be used as an external ADC input channel. Pull-up disabled.

Pin No.	Pin Name (After Reset)	Type	I/OStructure	Fail-safe Support	Optional Alternate Function		Note
					Alternate function	Optional function	
23	PA6	I/O	TTa	Yes	TIM1_BKIN/ TIM3_CH1/ TIM8_BKIN/ SPI1_MISO/ TIM13_CH1/ DCMI_PIXCLK	ADC_IN6/ OPA2_VINP	-
24	PA7	I/O	TTa	Yes	TIM1_CH1N/ TIM3_CH2/ TIM8_CH1N/ SPI1_MOSI/ TIM14_CH1/ ETH_RX_DV/ EVENTOUT	ADC_IN7/ OPA2_VINM	-
25	PC4	I/O	TTa	Yes	CLK1HZ/ TIM10_CH1/ USART7_CK/ ETH_RXD0	ADC_IN14/ ACMP2_INM	-
26	PC5	I/O	TTa	Yes	RTC_VLD_ON/ TIM10_CH2/ USART8_CTS/ ETH_RXD1	ADC_IN15/ ACMP2_INP	-

Pin No.	Pin Name (After Reset)	Type	I/OStructure	Fail-safe Support	Optional Alternate Function		Note
					Alternate function	Optional function	
27	PB0	I/O	TTa	Yes	TIM1_CH2N/ TIM3_CH3/ TIM8_CH2N/ TIM13_CH3/ ETH_RXD2	ADC_IN8/ OPA2_VOUT	-
28	PB1	I/O	TTa	Yes	TIM1_CH3N/ TIM3_CH4/ TIM8_CH3N/ TIM13_CH4/ ETH_RXD3/ EVENTOUT	ADC_IN9/ ACMP1_INM	-
29	PB2	I/O	TTa	Yes	TIM10_CH3/ TIM13_CH1	ACMP1_INP	BOOT1 as an input connected to pull-down resistor by default
30	PE7	I/O	FT	Yes	TIM1_ETR/ TIM14_CH2	-	-
31	PE14	I/O	FT	Yes	TIM1_CH4	-	-
32	PB10	I/O	FT	Yes	TIM2_CH3/ LPUART_RX/ I2C2_SCL/ SPI2_SCK/ I2S1_CK/ UART3_TX/ ETH_RX_ER	-	-

Pin No.	Pin Name (After Reset)	Type	I/OStructure	Fail-safe Support	Optional Alternate Function		Note
					Alternate function	Optional function	
33	PB11	I/O	FT	Yes	TIM2_CH4/ LPUART_TX/ I2C2_SDA/ UART3_RX/ ETH_TX_EN	-	-
34/55	V_{cap}	S	-	-	-	-	-
36	PB12	I/O	FT	Yes	TIM1_BKIN/ I2C2_SDA/ SPI2_NSS/ I2S1_WS/ UART6_CTS/ CAN2_RX/ TIM12_CH3/ ETH_TXD0/ EVENTOUT	-	-
37	PB13	I/O	FT	Yes	TIM1_CH1N/ SPI2_SCK/ I2S1_CK/ UART3_CTS/ UART6_RTS/ CAN2_TX/ TIM12_CH4/ ETH_TXD1	-	-

Pin No.	Pin Name (After Reset)	Type	I/OStructure	Fail-safe Support	Optional Alternate Function		Note
					Alternate function	Optional function	
38	PB14	I/O	FT	Yes	TIM1_CH2N/ TIM8_CH2N/ I2C2_SCL/ SPI2_MISO/ I2S1_EXTSD/ UART3_RTS/ TIM12_CH1	-	-
39	PB15	I/O	FT	Yes	TIM1_CH3N/ TIM8_CH3N/ I2C2_SDA/ SPI2_MOSI/ I2S1_SD/ TIM12_CH2	-	-
40	PD8	I/O	FT	Yes	UART3_TX/ TIM13_CH2/	-	-
41	PD9	I/O	FT	Yes	UART3_RX/ TIM13_CH3	-	-
42	PD10	I/O	FT	Yes	LPTIM2_IN/ TIM13_CH4	-	-
43	PD12	I/O	FT	Yes	TIM4_CH1/ UART3_RTS	-	-
44	PD13	I/O	FT	Yes	TIM4_CH4	-	-

Pin No.	Pin Name (After Reset)	Type	I/OStructure	Fail-safe Support	Optional Alternate Function		Note
					Alternate function	Optional function	
45	PC6	I/O	FT	Yes	TIM3_CH1/ TIM8_CH1/ I2S1_MCLK/ UART6_TX/ USART8_TX/ SDIO_D6/ DCMI_D0	-	-
46	PC7	I/O	FT	Yes	TIM3_CH2/ TIM8_CH2/ I2S2_MCLK/ UART6_RX/ USART8_RX/ SDIO_D7/ DCMI_D1/ EVENTOUT	-	-
47	PC8	I/O	FT	Yes	TIM3_CH3/ TIM8_CH3/ USART8_CK/ SDIO_D0/ DCMI_D2	-	-

Pin No.	Pin Name (After Reset)	Type	I/OStructure	Fail-safe Support	Optional Alternate Function		Note
					Alternate function	Optional function	
48	PC9	I/O	FT	Yes	MCO2/ TIM3_CH4/ TIM8_CH4/ I2C3_SDA/ USART8_RTS/ SDIO_D1/ DCMI_D3	-	-
49	PA8	I/O	FT	Yes	MCO1/ TIM1_CH1/ I2C3_SCL	-	-
50	PA9	I/O	FT	Yes	TIM1_CH2/ I2C3_SDA/ UART1_TX/ DCMI_D0	-	-
51	PA10	I/O	FT	Yes	TIM1_CH3/ UART1_RX/ DCMI_D1	-	-
52	PA11	I/O	TTa	-	TIM1_CH4/ UART1_CTS/ CAN1_RX	USB_DM	-

Pin No.	Pin Name (After Reset)	Type	I/OStructure	Fail-safe Support	Optional Alternate Function		Note
					Alternate function	Optional function	
53	PA12	I/O	TTa	-	TIM1_ETR/ UART1_RTS/ CAN1_TX/ EVENTOUT	USB_DP	-
54	PA13	I/O	FT	Yes	SWDIO-JTMS	-	Default SWDIO with an internal pull-up resistor
57	PA14	I/O	FT	Yes	SWCLK-JTCK	-	Default SWCLK with an internal pull-up resistor
58	PA15	I/O	FT	Yes	JTDI/ TIM2_CH1_ETR/ TIM10_CH2/ SPI1_NSS/ SPI3_NSS/ I2S2_WS	-	Default JTDI with an internal pull-up resistor
59	PC10	I/O	FT	Yes	TIM10_CH4/ I2S2_CK/ SPI3_SCK/ UART3_TX/ UART4_TX/ SDIO_D2/ DCMI_D8	-	-

Pin No.	Pin Name (After Reset)	Type	I/OStructure	Fail-safe Support	Optional Alternate Function		Note
					Alternate function	Optional function	
60	PC11	I/O	FT	Yes	TIM10_CH3/ I2S2_EXTSD/ SPI3_MISO/ UART3_RX/ UART4_RX/ SDIO_D3/ DCMI_D4	-	-
61	PC12	I/O	FT	Yes	I2C3_SCL/ I2S2_SD/ SPI3_MOSI/ UART5_TX/ SDIO_CK/ DCMI_D9/ EVENTOUT	-	-
62	PD0	I/O	FT	Yes	CAN1_RX	-	-
63	PD1	I/O	FT	Yes	CAN1_TX	-	-
64	PD2	I/O	FT	Yes	TIM3_ETR/ TIM11_CH2/ I2C3_SDA/ UART5_RX/ ETH_CLK125M_IN SDIO_CMD/ DCMI_D11	-	-

Pin No.	Pin Name (After Reset)	Type	I/OStructure	Fail-safe Support	Optional Alternate Function		Note
					Alternate function	Optional function	
65	PD7	I/O	FT	Yes	TIM13_CH1	-	-
66	PB3	I/O	FT	Yes	JTDO-TRACESWO/ TIM2_CH2/ SPI1_SCK/ SPI3_SCK/ I2S2_CK/ USART8_CK/ TIM13_CH2	-	Default JTDO，input floating
67	PB4	I/O	FT	Yes	NJRST/ TIM3_CH1/ SPI1_MISO/ SPI3_MISO/ I2S2_EXTSD/ USART8_TX/ SDIO_CD	-	Default NJRST, input, with an internal pull-down resistor

Pin No.	Pin Name (After Reset)	Type	I/OStructure	Fail-safe Support	Optional Alternate Function		Note
					Alternate function	Optional function	
68	PB5	I/O	FT	Yes	TIM3_CH2/ I2C1_SDA/ SPI1_MOSI/ SPI3_MOSI/ I2S2_SD/ USART8_RX/ CAN2_RX/ SDIO_WP/ DCMI_D10	-	-
69	PB6	I/O	FT	Yes	TIM4_CH1/ I2C1_SCL/ UART1_TX/ USART8_CTS/ CAN2_TX/ SDIO_RSTN/ DCMI_D5	-	-
70	PB7	I/O	FT	Yes	TIM4_CH2/ I2C1_SDA/ UART1_RX/ USART8_RTS/ DCMI_VSYNC/ EVENTOUT	-	-

Pin No.	Pin Name (After Reset)	Type	I/OStructure	Fail-safe Support	Optional Alternate Function		Note
					Alternate function	Optional function	
71	BOOT0	I	B	Yes	-	-	An external pull-up or pull-down resistor is required.
72	PB8	I/O	FT	Yes	TIM4_CH3/ TIM10_CH1/ I2C1_SCL/ CAN1_RX/ ETH_TXD3/ SDIO_D4/ DCMI_D6	-	-
73	PB9	I/O	FT	Yes	TIM4_CH4/ TIM11_CH1/ I2C1_SDA/ SPI2_NSS/ I2S1_WS/ CAN1_TX/ SDIO_D5/ DCMI_D7	-	-
74	PE0	I/O	FT	Yes	TIM4_ETR	-	-
76	PE3	I/O	FT	Yes	TIM9_CH3/ SPI4_SCK	-	-

Notes:

1. PC13, PC14, and PC15 are powered by a power switch. Due to the limited sink current capability of the switch (3 mA), the following limitations apply when using GPIO PC13 to PC15 in output mode:

   - The speed must not exceed 2 MHz, and the maximum load is 30 pF.
   - These IOs shall not be used as current sources (e.g., for driving LEDs).

2. When PA4 and PA5 are used as GPIOs, it is not recommended to enable the pull-up resistor function. When they are used as ADC input channels for sampling, it is necessary to ensure that the analog signal being sampled is strong, otherwise, it is not recommended to use them as ADC input channels.

3.3 Alternate Function

Table 3-3: Pin Alternate Function of Port A

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/ LPUART	TIM1/3/5	TIM8/9/10	I2C3	SPI1	SPI3	UART1/2/ I2S2	UART4 /I2S2	CAN1/USART7 /TIM13/14	QSPI	ETH	-	DCMI	-	EVENTOUT
Port A	PA0	-	TIM2_CH1_ETR	TIM5_CH1	TIM8_ETR	-	-	-	UART2_CTS	UART4_TX	USART7_CTS	-	ETH_CRS	-	-	-	-
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	UART2_RTS	UART4_RX	USART7_RTS	-	ETH_RX_CLK (ETH_REF_50M)	-	-	-	EVENTOUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	UART2_TX	UART4_CTS	USART7_TX	-	ETH_MDIO	-	-	-	-
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	-	UART2_RX	UART4_RTS	USART7_RX	-	ETH_COL	-	-	-	-
	PA4	-	LPUART_TX	TIM1_CH3	-	-	SPI1_NSS	SPI3_NSS	-	I2S2_WS	USART7_CK	-	-	-	DCMI_HSYNC	-	-
	PA5	-	TIM2_CH1_ETR	TIM1_CH4	TIM8_CH1N	-	SPI1_SCK	-	-	-	TIM13_CH2	-	-	-	-	-	-
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	-	-	-	TIM13_CH1	-	-	-	DCMI_PIXCK	-	-
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI	-	-	-	TIM14_CH1	-	ETH_RX_DV	-	-	-	EVENTOUT
	PA8	MCO1	TIM1_CH1	-	-	I2C3_SCL	-	-	-	-	-	-	-	-	-	-	-
	PA9	-	TIM1_CH2	-	-	I2C3_SDA	-	-	UART1_TX	-	-	-	-	-	DCMI_D0	-	-
	PA10	-	TIM1_CH3	-	-	-	-	-	UART1_RX	-	-	-	-	-	DCMI_D1	-	-
	PA11	-	TIM1_CH4	-	-	-	-	-	UART1_CTS	-	CAN1_RX	-	-	-	-	-	-
	PA12	-	TIM1_ETR	-	-	-	-	-	UART1_RTS	-	CAN1_TX	-	-	-	-	-	EVENTOUT
	PA13	JTMS SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PA14	JTCK SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PA15	JTDI	TIM2_CH1_ETR	-	TIM10_CH2	-	SPI1_NSS	SPI3_NSS	I2S2_WS	-	-	-	-	-	-	-	-

Table 3-4: Pin Alternate Function of Port B

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/ LPUART	TIM8/10/11	I2C1/2	SPI1/SPI2	SPI3/I2S1	UART1/3/ I2S2	UART6 USART8	CAN1/2/ TIM12/13	TIM12/ QSPI	ETH	EMC/ SDIO	DCMI	-	EVENTOUT
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	-	-	-	TIM13_CH3	-	ETH_RXD2	-	-	-	-
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	-	-	-	TIM13_CH4	-	ETH_RXD3	-	-	-	EVENTOUT
	PB2	-	-	-	TIM10_CH3	-	-	-	-	-	TIM13_CH1	-	-	-	-	-	-
	PB3	JTDO/ TRACESWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK	I2S2_CK	USART8_CK	TIM13_CH2	-	-	-	-	-	-
	PB4	NJTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	I2S2_EXTSD	USART8_TX	-	-	-	SDIO_CD	-	-	-
	PB5	-	-	TIM3_CH2	-	I2C1_SDA	SPI1_MOSI	SPI3_MOSI	I2S2_SD	USART8_RX	CAN2_RX	-	-	SDIO_WP	DCMI_D10	-	-
	PB6	-	-	TIM4_CH1	-	I2C1_SCL	-	-	UART1_TX	USART8_CTS	CAN2_TX	-	-	SDIO_RSTN	DCMI_D5	-	-
	PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	UART1_RX	USART8_RTS	-	-	-	-	DCMI_VSYNC	-	EVENTOUT
	PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	-	-	-	CAN1_RX	-	ETH_TXD3	SDIO_D4	DCMI_D6	-	-
	PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS	I2S1_WS	-	-	CAN1_TX	-	-	SDIO_D5	DCMI_D7	-	-
	PB10	-	TIM2_CH3	LPUART_RX	-	I2C2_SCL	SPI2_SCK	I2S1_CK	UART3_TX	-	-	QSPI_SCK	ETH_RX_ER	EMC_A0	-	-	-
	PB11	-	TIM2_CH4	LPUART_TX	-	I2C2_SDA	-	-	UART3_RX	-	-	-	ETH_TX_EN	EMC_A1	-	-	-
	PB12	-	TIM1_BKIN	-	-	I2C2_SDA	SPI2_NSS	I2S1_WS	-	UART6_CTS	CAN2_RX	TIM12_CH3	ETH_TXD0	EMC_A2	-	-	EVENTOUT
	PB13	-	TIM1_CH1N	-	-	-	SPI2_SCK	I2S1_CK	UART3_CTS	UART6_RTS	CAN2_TX	TIM12_CH4	ETH_TXD1	EMC_A3	-	-	-
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	I2C2_SCL	SPI2_MISO	I2S1_EXTSD	UART3_RTS	-	TIM12_CH1	-	-	-	-	-	-
	PB15	-	TIM1_CH3N	-	TIM8_CH3N	I2C2_SDA	SPI2_MOSI	I2S1_SD	-	-	TIM12_CH2	-	-	-	-	-	-

Table 3-5: Pin Alternate Function of Port C

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	LPUART/ LPTIM1~2	TIM3/5	TIM8/10	I2C3	SPI2/ I2S1/2	SPI3/ I2S1/2	UART3	UART4/5/ 6	USART7/8	-	ETH	EMC/ SDIO	DCMI	-	EVENTOUT
Port C	PC0	-	LPTIM1_IN	TIM5_CH1	-	-	-	-	-	-	USART7_CTS	-	-		-	-	-
	PC1	-	LPTIM1_OUT	TIM5_CH2	-	-	-	-	-	-	USART7_RTS	-	ETH_MDC		-	-	EVENTOUT
	PC2	-	LPUART_RX	TIM5_CH3	-	-	SPI2_MISO	I2S1_EXTSD	-	-	USART7_TX	-	ETH_TXD2		-	-	-
	PC3	-	LPTIM1_TRIG	TIM5_CH4	-	-	SPI2_MOSI	I2S1_SD	-	-	USART7_RX	--	ETH_TX_CLK		-	-	-
	PC4	CLK1HZ	-	-	TIM10_CH1	-	-	-	-	-	USART7_CK	-	ETH_RXD0		-	-	-
	PC5	RTC_VLD_ON	-	-	TIM10_CH2	-	-	-	-	-	USART8_CTS	-	ETH_RXD1		-	-	-
	PC6	-	-	TIM3_CH1	TIM8_CH1	-	I2S1_MCLK	-	-	UART6_TX	USART8_TX	-	-	SDIO_D6	DCMI_D0	-	-
	PC7	-	-	TIM3_CH2	TIM8_CH2	-	-	I2S2_MCLK	-	UART6_RX	USART8_RX	-	-	SDIO_D7	DCMI_D1	-	EVENTOUT
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	-	-	USART8_CK	-	-	SDIO_D0	DCMI_D2	-	-
	PC9	MCO2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	-	-	-	-	USART8_RTS	-	-	SDIO_D1	DCMI_D3	-	-
	PC10	-	-	-	TIM10_CH4	-	I2S2_CK	SPI3_SCK	UART3_TX	UART4_TX	-	-	-	SDIO_D2	DCMI_D8	-	-
	PC11	-	-	-	TIM10_CH3	-	I2S2_EXTSD	SPI3_MISO	UART3_RX	UART4_RX	-	-	-	SDIO_D3	DCMI_D4	-	-
	PC12	-	-	-	-	I2C3_SCL	I2S2_SD	SPI3_MOSI	-	UART5_TX	-	-	-	SDIO_CK	DCMI_D9	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Table 3-6: Pin Alternate Function of Port D

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		-	LPTIM2	TIM3/4	TIM11	I2C2	-	-	UART2/3	UART5	CAN1/TIM13	QSPI	ETH	EMC/ SDIO	DCMI	-	EVENTOUT
Port D	PD0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	-	-	-	-	-
	PD1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	-	-	-	-	-
	PD2	-	-	TIM3_ETR	TIM11_CH2	I2C3_SDA	-	-	-	UART5_RX	-	-	ETH_CLK125M_IN	SDIO_CMD		-	-
	PD7	-	-	-	-	-	-	-	-	-	TIM13_CH1	-	-	-	-	-	-
	PD8	-	-	-	-	-	-	-	UART3_TX	-	TIM13_CH2	-	-	-	-	-	-
	PD9	-	-	-	-	-	-	-	UART3_RX	-	TIM13_CH3	-	-	-	-	-	-
	PD10	-	LPTIM2_IN	-	-	-	-	-		-	TIM13_CH4	-	-	-	-	-	-
	PD12	-	-	TIM4_CH1	-	-	-	-	UART3_RTS	-	-	-	-	-	-	-	-
	PD13	-	-	TIM4_CH2	-	-	-	-	-	-	-	-	-	-	-	-	-
	PD8	-	-	-	-	-	-	-	UART3_TX	-	TIM13_CH2	-	-	-	-	-	-

Table 3-7: Pin Alternate Function of Port E

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/LPTIM2	TIM4	TIM9	-	-	SPI4	-	-	TIM14	QSPI	ETH	EMC	DCMI	-	EVENTOUT
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-	-	-	-	-	-	-	-	-
	PE3	-	-	-	TIM9_CH3	-	-	SPI4_SCK			-	-	-	-	-	-	-
	PE4	-	-	-	TIM9_CH4	-	-	SPI4_NSS			-	-	-	-	-	-	-
	PE5	TRACED2	-	-	TIM9_CH1	-	-	SPI4_MISO	-	-	-	-	-	-	DCMI_D6	-	-
	PE6	-	-	-	TIM9_CH2	-	-	SPI4_MOSI			-	-	-	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-	-	-	-	TIM14_CH2	-	-	-	-	-	EVENTOUT
	PE14	-	TIM1_CH4	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Table 3-8: Pin Alternate Function of Port H

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

4 Electrical Characteristics

4.1 Test Condition

Unless otherwise specified, all voltages are referenced to V_{ss}.

4.1.1 Minimum and Maximum Values

Unless otherwise specified, all products are tested on the production line at T_A=25℃. The maximum and minimum values support the worst-case environmental temperature, supply voltage, and clock frequency as specified.

Notes below each table indicate that data are obtained through comprehensive evaluation, design simulation, or process characteristics, and not tested on the production line. Based on comprehensive evaluation, the maximum and minimum values are derived from sample testing by taking the average value and adding or subtracting three times the standard deviation (average ± 3σ).

4.1.2 Typical Value

Unless otherwise specified, typical data are measured based on T_A = 25 ℃ and V_{DDH} = V_{DDA} = 3.3 V. They are given only as design guidelines.

4.1.3 Typical Curve

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.1.4 Power Supply Scheme

The chip supports single power supply and VBAT backup power supply. It requires an external operating supply voltage between 1.8 V and 3.6 V, and a digital circuit operating voltage generated by the built-in LDO.

The system power supply scheme is shown below.

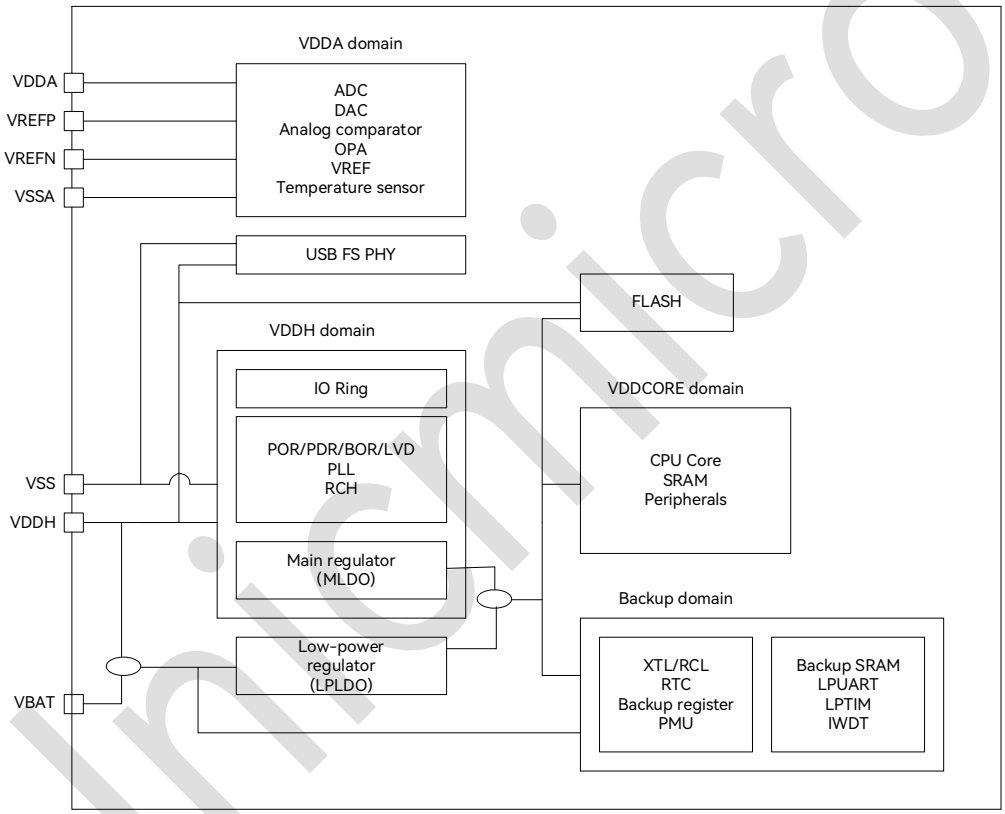


Figure 4-1: Block Diagram of Power Supply Scheme

4.2 Absolute Maximum Ratings

Stresses above the absolute maximum ratings listed in Table 4-1, Table 4-2 and Table 4-3 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1: Voltage Characteristics

Symbol	Description	Min.	Max.	Unit
V_{DDH} – V_{SS}	External main supply voltage (including V_{DDA} and V_{DDH}) (1)	-0.3	4	V
V_{IN}	Input voltage on 5 V tolerant pin (3)	V_{SS}-0.3	5.5	
	Input voltage on other pins (2)	V_{SS}-0.3	V_{DDH}+0.3	
$\|\Delta V_{DDx}\|$	Voltage difference between different supply pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Voltage difference between different ground pins	-	50	

Notes:

1. All power supply (V_{DDH}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to an external power supply system in the permitted range.

2. V_{IN} shall not exceed its maximum value. Refer to Table 4-2 for current characteristics.

3. When a 5.5 V voltage is applied to the 5 V tolerant pin, V_{DDH} must not be lower than 2.25 V.

Table 4-2: Current Characteristics

Symbol	Description	Max. (1)	Unit
I_{VDDH}	Total current through the V_{DDH}/V_{DDA} power lines (supply current) (1) (3)	200	mA
I_{VSS}	Total current through the V_{SS} ground lines (sink current) (1) (3)	200	
I_{IO}	Output sink current on any I/O and control pins	12	
	Output current on any I/O and control pins	-12	
$I_{INJ(PIN)}$(2)	Injection current on NRST pin	-5	
	Injection current on other pins	±5	

Notes:

1. All power supply (V_{DDH}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to an external power supply system in the permitted range.

2. When V_{IN} > V_{DDH}, there is a forward injection current; when VIN < VSS, there is a reverse injection current. $I_{INJ(PIN)}$ shall not exceed its maximum value. Refer to Table 4-1 for voltage characteristics.

3. When the maximum current occurs, the maximum allowable voltage drop for V_{DDH} is 0.1 × V_{DDH}.

Table 4-3: Temperature Characteristics

Symbol	Description	Value	Unit
T_{stg}	Storage temperature range	-40~+150	℃
T_J	Maximum junction temperature	125	℃

4.3 Operating Condition

Static parameter table (applicable temperature range: T_A = -40℃~+105℃).

4.3.1 General Operating Condition

Table 4-4: General Operating Condition

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	240	288	MHz
f_{PCLK0}	Internal APB0 clock frequency	-	0	120	144	
f_{PCLK1}	Internal APB1 clock frequency	-	0	240	288	
f_{PCLK2}	Internal APB2 clock frequency	-	0	240	288	
f_{PCLK3}	Internal APB3 clock frequency	-	0	60	72	
V_{DDH}	Standard operating voltage	-	1.8	-	3.6	V
V_{DDA}	Analog section operating voltage	Must be the same as V_{DDH} voltage	1.8	-	3.6	V
T_A	Ambient temperature	-	-40	-	105	℃
T_J	Junction temperature range	-	-40	-	125	℃

Note: It is recommended to use the same power supply for V_{DDH} and V_{DDA}. During power-up and normal operation, the maximum allowable difference between V_{DDH} and V_{DDA} is 300 mV.

4.3.2 Operating Condition at Power-up / Power-down

Table 4-5: Operating Condition at Power-up / Power-down

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{VDDH}	V_{DDH} rise time	The power supply voltage rises from 0 to V_{DDH}.	20	∞	μs/V
	V_{DDH} fall time	The power supply voltage falls from V_{DDH} to 0.	80	∞	

4.3.3 Characteristics of Embedded Reset and Power Control Module

Table 4-6: Characteristics of Embedded Reset and Power Control Module

Symbol	Type	Condition	Typical Voltage	Unit
V_{PDR}	PDR rising trigger point	PDRS[1:0] = 00	1.57	V
		PDRS[1:0] = 01	1.77	
		PDRS[1:0] = 10	1.87	
		PDRS[1:0] = 11	1.97	
	PDR falling trigger point	PDRS[1:0] = 00	1.49	
		PDRS[1:0] = 01	1.67	
		PDRS[1:0] = 10	1.77	
		PDRS[1:0] = 11	1.87	
	Hysteresis voltage of PDR trigger point	PDRS[1:0] = 00	0.08	
		PDRS[1:0] = 01	0.1	
		PDRS[1:0] = 10	0.1	
		PDRS[1:0] = 11	0.1	
V_{BOR}	BOR trigger point	BORS[3:0] = 0000	1.56	V
		BORS[3:0] = 0001	1.66	
		BORS[3:0] = 0010	1.75	
		BORS[3:0] = 0011	1.85	
		BORS[3:0] = 0100	1.95	
		BORS[3:0] = 0101	2.05	
		BORS[3:0] = 0110	2.14	
		BORS[3:0] = 0111	2.24	
		BORS[3:0] = 1000	2.34	

Symbol	Type	Condition	Typical Voltage	Unit
		BORS[3:0] = 1001	2.43	
		BORS[3:0] = 1010	2.53	
		BORS[3:0] = 1011	2.63	
		BORS[3:0] = 1100	2.73	
		BORS[3:0] = 1101	2.83	
		BORS[3:0] = 1110	2.92	
		BORS[3:0] = 1111	3.02	
V_{LVD}	LVD trigger point	LVDS[3:0] = 0000	1.59	V
		LVDS[3:0] = 0001	1.68	
		LVDS[3:0] = 0010	1.78	
		LVDS[3:0] = 0011	1.88	
		LVDS[3:0] = 0100	1.98	
		LVDS[3:0] = 0101	2.08	
		LVDS[3:0] = 0110	2.18	
		LVDS[3:0] = 0111	2.28	
		LVDS[3:0] = 1000	2.38	
		LVDS[3:0] = 1001	2.48	
		LVDS[3:0] = 1010	2.58	
		LVDS[3:0] = 1011	2.67	
		LVDS[3:0] = 1100	2.77	
		LVDS[3:0] = 1101	2.87	
		LVDS[3:0] = 1110	2.97	
		LVDS[3:0] = 1111	3.07	

Note: Guaranteed by design, not tested in production.

4.3.4 Supply Current Characteristics

Table 4-7: Supply Current Characteristics

Symbol	Parameter	Condition	f_{HCLK} (MHz)	Max.				Unit
				T_A = -40 ℃	T_A = 25 ℃	T_A = 85 ℃	T_A = 105 ℃	
I_{DD}	Supply current in run mode	All peripherals enabled, running while (1) + memcopy in flash	288	63.0	68.2	86.1	97.2	mA
			240	60.3	65.3	82.4	93.1	
			204	58.03	61.76	76.44	87.04	
			168	48.26	51.74	66.13	76.71	

Symbol	Parameter	Condition	f_{HCLK} (MHz)	Max.				Unit
				T_A = -40 ℃	T_A = 25 ℃	T_A = 85 ℃	T_A = 105 ℃	
			150	43.31	46.71	61.03	71.53	
			144	41.82	45.21	59.46	69.99	
			120	35.43	38.58	52.70	63.11	
			90	27.08	30.10	43.99	54.35	
			60	18.95	21.69	35.38	45.58	
			48	15.80	18.49	32.06	42.28	
			24	9.30	11.78	25.18	35.33	
			16	7.12	9.57	22.95	33.12	
			12	6.05	8.45	21.74	31.85	
		All peripherals disabled, only EFC enabled, running while (1) + memcopy in flash	288	20.3	26.2	41.1	55.1	
			240	18.2	23.9	38.2	50.3	
			204	16.72	19.90	33.92	44.33	
			168	13.96	17.06	30.96	41.41	
			150	12.63	15.65	29.53	39.89	
			144	12.32	15.34	29.21	39.64	
			120	10.55	13.52	27.38	37.69	
			90	8.12	11.09	24.84	35.14	
			60	5.85	8.73	22.44	32.67	
			48	4.64	7.50	21.15	31.39	
			24	2.84	5.64	19.20	29.46	
			16	2.24	5.01	18.58	28.84	
			12	1.93	4.71	18.26	28.48	

Notes:

1. APB1 = APB2 = 1/2 AHB, APB0 = APB3 = 1/4 AHB.
2. f_{HCLK} > 48 MHz is derived from PLL0 multiplication and f_{HCLK} ≤ 48 MHz is derived from RCH division.

Table 4-8: Typical Value in Low-power Mode

Symbol	Parameter	Condition	Typical Value			Unit
			T_A = -40 ℃	T_A = 25 ℃	T_A = 105 ℃	
I_{DD_Stop}	Supply current in Stop mode	Low-speed clock is enabled, RTC is running, independent watchdog is enabled, and high-frequency clocks PLL / XTH / RCH are stopped. CPU, IO, SRAM, etc. are retained, and the program before wake-up (low-voltage operation) can be continued after rapid wake-up.	-	1	-	mA
$I_{DD\_Standby0}$	Supply current in Standby0 mode	External low-speed clock is enabled, RTC is running, backup registers and 4 KB backup SRAM are retained, independent watchdog is enabled, LPTIM1/LPTIM2 and LPUART are disabled.	-	4.2	-	μA
		External low-speed clock is enabled, RTC is running, backup registers and 4 KB backup SRAM are retained, independent watchdog is disabled, LPTIM1/LPTIM2 and LPUART are disabled.	-	4	-	μA
		Internal low-speed clock is enabled, RTC is running, backup registers and 4 KB backup SRAM	-	3.81	-	μA

Symbol	Parameter	Condition	Typical Value			Unit
			T_A = -40 ℃	T_A = 25 ℃	T_A = 105 ℃	
		are retained, independent watchdog is disabled, LPTIM1/LPTIM2 and LPUART are disabled.				
$I_{DD\_Standby1}$	Supply current in Standby1 mode	External low-speed clock is enabled, RTC is running, backup registers are retained, 4 KB backup SRAM is not retained, independent watchdog is disabled, LPTIM1/LPTIM2 and LPUART are disabled.	-	2.17	-	μA
		Internal low-speed clock is enabled, RTC is running, backup registers are retained, 4 KB backup SRAM is not retained, independent watchdog is disabled, LPTIM1/LPTIM2 and LPUART are disabled.	-	1.98	-	μA
$I_{DD\_DeepStandby0}$	Supply current in DeepStandby0 mode	Both external and internal low-speed clocks are disabled, RTC does not run, backup registers and 4-KB backup SRAM are retained, independent watchdog is disabled. Powered by V_{DDH}	-	3.34	-	μA
$I_{DD\_DeepStandby1}$	Supply current in DeepStandby1 mode	Both external and internal low-speed clocks are disabled, RTC does	-	1.59	-	μA

Symbol	Parameter	Condition	Typical Value			Unit
			T_A = -40 ℃	T_A = 25 ℃	T_A = 105 ℃	
		not run, backup registers are retained, 4 KB backup SRAM is not retained, and independent watchdog is disabled. Powered by V_{DDH}				
$I_{DD\_DeepStandby1}$ (VBAT)	Supply current in DeepStandby1 mode	Both external and internal low-speed clocks are disabled, RTC does not run, backup registers are retained, 4 KB backup SRAM is not retained, and independent watchdog is disabled. V_{DDH} switched off; powered by V_{BAT}.	-	1.11	-	μA

4.3.5 External Clock Source Characteristics

4.3.5.1 External High-speed Clock Source (HSE / XTH)

Table 4-9: HSE/XTH Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{XTH_IN}	Oscillator frequency	XTH_SF[1:0] = 00	1	-	4	MHz
		XTH_SF[1:0] = 01	4.1	-	12	
		XTH_SF[1:0] = 10	12.1	-	24	
		XTH_SF[1:0] = 11	24.1	-	48	

Notes:

1. The resonator characteristics are given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design rather than test in production.

4.3.5.2 External Low-speed Clock Source (LSE/XTL)

Table 4-10: LSE/XTL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{XTL_IN}	Oscillator frequency	-	-	32.768	-	kHz
$t_{SU(XTL)}$	Startup time	V_{DDH} is stabilized	-	500	-	ms
I_{DD}	Operating current	-	-	200	-	nA
$C_{L1/CL2}$	External capacitance	-	-	20	-	pF

4.3.6 Internal Clock Source Characteristics

4.3.6.1 High-speed Internal RC Oscillator (RCH)

Table 4-11: RCH Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{RCH}	Frequency	V_{DDH} = 3.3 V, T_A = 25℃, after calibration	-	48	-	MHz
ACC_{RCH}	Accuracy of RCH oscillator	V_{DDH} = 3.3 V, T_A = -40~105℃	-1.5	-	2	%
$t_{SU(RCH)}$	Startup time of RCH oscillator	-	-	16	-	μs
$I_{DD(RCH)}$	Current consumption of RCH oscillator	-	-	80	-	μA

4.3.6.2 Low-speed Internal RC Oscillator (RCL)

Table 4-12: RCL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{RCL}	Frequency	V_{DDH} = 3.3 V, T_A = 25℃, after calibration	-	32	-	kHz
ACC_{RCL}	Accuracy of RCL oscillator	V_{DDH} = 3.3 V T_A = -40~105℃	-1.5	-	2	%
$t_{SU(RCL)}$	Startup time of RCL oscillator	-	-	-	500	μs
$I_{DD(RCL)}$	Current consumption of RCL oscillator	-	-	200	-	nA

4.3.7 Wake-up Time from Low-power Mode

Table 4-13: Wake-up Time

Symbol	Parameter	Typical Value	Unit
$t_{WUSleep}$	Wake-up time from Sleep mode	5	HCLK
t_{WUStop}	Wake-up time from Stop mode	3	μs
$t_{WUStandby0}$	Wake-up time from Standby0 mode	320	μs
$t_{WUStandby1}$	Wake-up time from Standby1 mode	410	μs

4.3.8 PLL Characteristics

Table 4-14: PLL Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{PLL_IN}	PLL reference input clock	0.9	-	100	MHz
	PLL input clock duty cycle	40	50	60	-
f_{VCO_OUT}	VCO output clock	300	-	600	MHz
f_{PLL_OUT}	PLL output clock ($f_{VCO\_OUT/P}$)	42.9	-	600	MHz
t_{LOCK}	PLL lock time (input reference clock 4 MHz)	-	-	150	μs
Jitter	RMS (cycle-to-cycle jitter) @ PLL clock output 240 MHz (integer mode)	-	15	-	ps
Jitter	RMS (cycle-to-cycle jitter) @ PLL clock output 240 MHz (fractional mode or spread-spectrum mode)	-	18	-	ps
I_{PLL}	Operating current of PLL	-	-	0.5	mA

Notes:

1. Guaranteed by design, not tested in production.

2. Fractional frequency division can be used for audio and other applications.

3. Spread-spectrum function helps to reduce electromagnetic interference.

4.3.9 Flash Memory Characteristics

Table 4-15: Flash Memory Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{prog}	32-bit programming time	-	41	-	μs
t_{ERASE}	Page (8K bytes) erase time	-	12	16	ms
t_{ME}	Mass erase time	-	-	16	ms
N_{END}	Endurance (erase count)	-	-	10	kcycle
t_{RET}	Data retention period	-	-	10	years

Note: Guaranteed by characterization test results, not tested in production.

4.3.10 Absolute Maximum Ratings (Electrical Sensitivity)

Using specific measurement methods, the chip is stressed to determine its performance in terms of electrical sensitivity.

4.3.10.1 Static Latch-up (LU)

Table 4-16: Electrical Sensitivity

Symbol	Parameter	Condition	Type
LU	Static latch-up class	T_A = +105℃, conforming to JESD78E	Class II A

4.3.11 I/O Port Characteristics

Table 4-17: I/O DC Characteristics at 3.3 V V_{DDH}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	-	V_{SS}	-	0.8	V
V_{IH}	Input high voltage	-	2	-	V_{DDH}	
V_{OL}	Output low voltage	-	V_{SS}	-	0.4	
V_{OH}	Output high voltage	-	2.4	-	V_{DDH}	
V_{hys}	Schmitt trigger hysteresis voltage	-	200	-	-	mV

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{lkg}	Input leakage current	V_{DDH} = Maximum V_{PAD} = 0 or V_{PAD} = V_{DDH}	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistance	V_{DDH} = 3.3 V, V_{IN} = V_{SS}	9	-	19.4	kΩ
R_{PD}	Weak pull-down equivalent resistance	V_{DDH} = 3.3 V, V_{IN} = V_{DDH}	6.7	-	16	kΩ

Table 4-18: I/O DC Characteristics at 1.8 V V_{DDH}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	-	V_{SS}	-	0.3*V_{DDH}	V
V_{IH}	Input high voltage	-	0.7*V_{DDH}	-	V_{DDH}	
V_{OL}	Output low voltage	-	V_{SS}	-	0.2*V_{DDH}	
V_{OH}	Output high voltage	-	0.8*V_{DDH}	-	V_{DDH}	
V_{hys}	Schmitt trigger hysteresis voltage	-	0.1*V_{DDH}	-	-	mV
I_{lkg}	Input leakage current	V_{DDH} = Maximum V_{PAD} = 0 or V_{PAD} = V_{DDH}	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistance	V_{DDH} = 3.3 V, V_{IN} = V_{SS}	11.2	-	32.4	kΩ
R_{PD}	Weak pull-down equivalent resistance	V_{DDH} = 3.3 V, V_{IN} = V_{DDH}	9.4	-	32.4	kΩ

4.3.12 ADC Electrical Characteristics

Table 4-19: ADC Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	Using external reference voltage	1.8	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	-	0	-	V
f_{ADC}	ADC clock frequency	-	-	-	84	MHz
f_s	Sampling rate	1.8 V ≤ V_{DDA} ≤ 3.6 V	-	-	5.25	Msps
Resolution	Resolution	-	-	12	-	bit
V_{AIN}	Conversion voltage range	-	0	-	V_{REF+}	V
C_{IN}	Input capacitance	-	-	6	-	pf

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SNR	Signal-to-noise-and-distortion ratio	SNR @ 30 kHz	-	64	-	dB
THD	-	THD @ 30 kHz	-	-65	-	dB
DNL	-	DNL	-1	±0.6	1.5	LSB
INL	-	INL	-3	±1.5	2	LSB
ENOB	-	ENOB @ 30 kHz	-	10	-	Bits

Note: Guaranteed by design, not tested in production.

4.3.13 DAC Electrical Characteristics

Table 4-20: DAC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	1.8	3.3	3.6	V
RL	Load resistance with buffer enabled	5	-	-	kΩ
CL	Load capacitance	-	-	50	pF
DAC_OUT	DAC_OUT voltage with buffer disabled	0	-	V_{REF+}	V
	DAC_OUT voltage with buffer enabled	0.2	-	V_{REF+}-0.2	V
V_{REF+}	-	TYP-0.1%	1.5/2.0/2.5/3.0 or V_{DDA}	TYP+0.1%	V
V_{REF-}	-	-	-	0	V
Resolution	Resolution	-	12	-	bit
F_S	Sampling rate	-	-	1	MHz
SNR	-	-	65	-	dB
THD	-	-	65	-	dB
DNL	Differential non linearity	-	2	-	LSB
INL	Integral non linearity	-	4	-	LSB

Note: Guaranteed by design, not tested in production.

4.3.14 Operational Amplifier (OPA) Characteristics

Table 4-21: OPA Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DDA}	Operating voltage	1.8	-	3.6	V
T_A	Ambient temperature	-40	-	105	℃
I_{DDA}	Operating current	-	5	-	mA
C_{MIR}	Common mode input range	0	-	V_{DDA}	V
R_{LOAD}	Load resistance	600	-	-	Ω
C_{LOAD}	Load capacitance	-	6	30	pF
Mode	OPA mode supported Comparator mode Unit buffer mode PGA mode	-	-	-	-

Note: Guaranteed by design, not tested in production.

4.3.15 Analog Comparator (ACMP) Electrical Characteristics

Table 4-22: ACMP Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{IN}	Input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	-	10	μs
t_{DR}	Comparator rising-edge propagation delay	V_{DDA} = 3.3 V, V_{IN} = 5 mV	0.8	-	2.6	μs
t_{DF}	Comparator falling-edge propagation delay	V_{DDA} = 3.3 V, V_{IN} = 5 mV	6.7	-	17.9	μs
V_{OFFSET}	Comparator input offset error		-	-	±10	mV
V_{hys}	Comparator hysteresis voltage	CHYS[1:0] = 00	-	0	-	mV
		CHYS[1:0] = 01	-	10.5	-	mV
		CHYS[1:0] = 10	-	20.5	-	mV
		CHYS[1:0] = 11	-	30.5	-	mV
I_{DDA}	Operating current	Normal operation (CEN = 1, CLPM = 0)	-	-	5	μA

Note: Guaranteed by design, not tested in production.

4.3.16 Temperature Sensor (TS) Characteristics

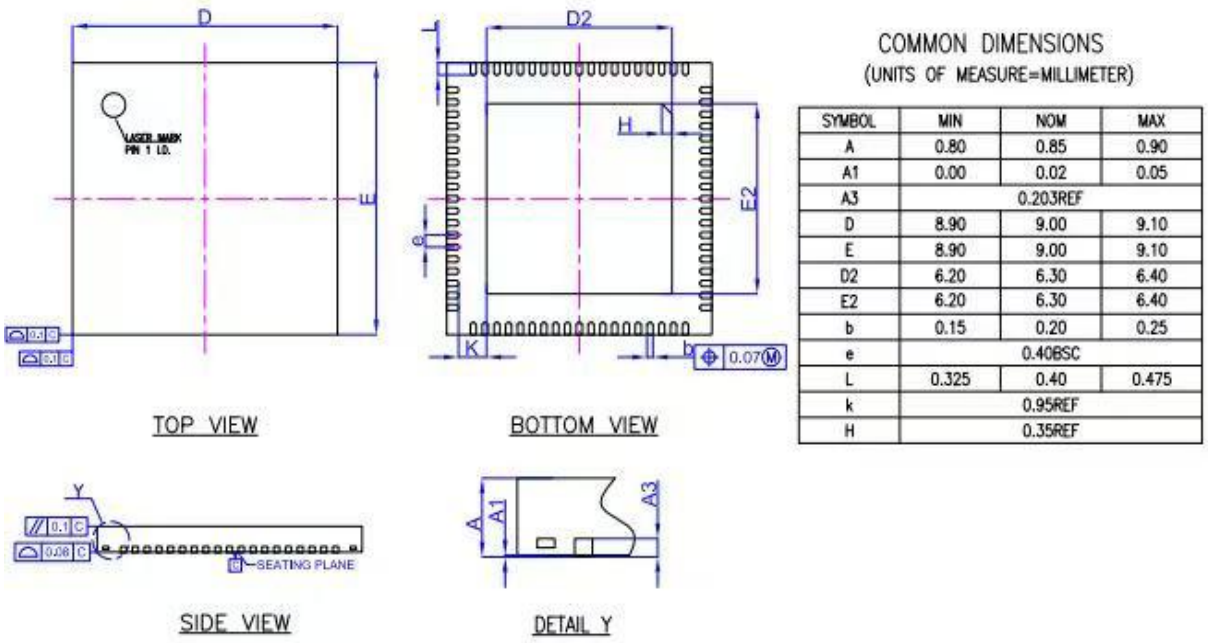
Table 4-23: Temperature Sensor Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_L	Linearity with respect to temperature	-	±1	±3	°C
t_{START}	Start-up time	-	10	-	μs

Note: Guaranteed by characterization test results, not tested in production.

5 Package Outline

5.1 QFN76 (9 * 9 mm)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203REF	
D	8.90	9.00	9.10
E	8.90	9.00	9.10
D2	6.20	6.30	6.40
E2	6.20	6.30	6.40
b	0.15	0.20	0.25
e		0.40BSC	
L	0.325	0.40	0.475
k		0.95REF	
H		0.35REF	

Figure 5-1: QFN76 Package Outline Drawing

6 Revision History

Date	Version	Description
May-30-2026	V1.0.0	Initial release.

7 Contact Us

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