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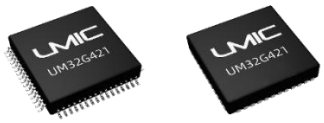
UM32G421

High-performance Low-power 32-bit MCU: ARM® Cortex®-M4 (FPU + DSP), 256 KB eFlash, 64 KB SRAM, USB FS, Encryption/Decryption Engines, 17 Timers, RTC, 2 ADCs, 1 DAC, Rich Communication Interfaces

Product Features

- **Low power management system**
  - 1.5 µA @ 3.3 V Standby mode, RTC running
  - 70 µA/MHz @ 3.3 V @ 204 MHz Run mode
  - Integrated RTC, LPTIM, IWDT and LPUART
  - Low power modes: Sleep, Stop, Standby and DeepStandby
  - Optional VBAT supply for RTC and 20 x 32-bit backup registers + optional 8KB backup SRAM
- **Processor**
  - 32-bit ARM® Cortex®-M4
  - Integrated single-precision floating-point unit (FPU)
  - Integrated hardware DSP instruction unit
  - Memory protection unit (MPU)
  - Three-stage pipeline, main frequency up to 204 MHz in boost mode
  - Single-cycle hardware multiplier
  - CPU performance reaches 255 DMIPS (1.25 DMIPS/MHz, 204 MHz)
  - CoreMark score as high as 702 (3.445 CoreMark/MHz, 204 MHz)
  - 2KB instruction Cache, supporting 0-wait-state instruction fetch
- **Memory**
  - 64KB SRAM, of which 8KB can be used as retention SRAM
  - 256KB eFlash
- **GPIO**
  - Up to 54 I/O ports with interrupt capability
  - Up to 28 I/Os with 5V tolerance



LQFP64 (10*10mm)
LQFP64 (7*7mm)
LQFP48 (7*7mm)

QFN48 (6*6mm)
QFN40 (5*5mm)
QFN32 (4*4mm)

- **Reset and power management**
  - Power-on reset (POR) / power-down reset (PDR) / low-voltage detection (LVD) / brown-out reset (BOR)
- **Clock**
  - Crystal oscillator from 1 MHz to 48 MHz
  - Built-in 96 MHz RC oscillator (±1% accuracy at 0 ~ 85 ℃)
  - 32.768 kHz crystal oscillator with calibration function
  - Built-in low-frequency 32 kHz RC oscillator (±1% accuracy at room temperature)
  - 1 x PLL (supporting integer, fractional and spread spectrum functions)
- **Communication interfaces**
  - Up to 4 UART interfaces, including 3 standard UARTs and 1 enhanced UART (UART1 supports flow control, 7/8/9 data bits, up to 10.5 Mbps, IrDA control, and DMA acceleration)
  - 2 USART interfaces, supporting UART/SPI/IrDA/LIN functions, with DMA acceleration
  - 2 x LPUART interfaces, supporting up to 9,600 bps in low-power mode and up to 115,200 bps in high-speed mode
  - 3 x I2C interfaces (up to 1 Mbps), supporting master/slave modes, 7-bit/10-bit addressing. Wherein I2C0 is a standard I2C, while I2C1/2 are enhanced I2Cs, supporting SMBus and

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DMA operations.

- 1 x I2S interface, supporting I2S/PCM formats, and master/slave modes
- Up to 3 x SPI interfaces (supporting up to 60 MHz), master/slave modes, Mode 0/1/2/3 protocols. SPI2 is an enhanced SPI, supporting data sizes from 4 bits to 32 bits, with DMA acceleration.
- Up to 37 PWM output channels
- 1 x CAN industrial bus, supporting CANFD, and compatible with CAN2.0A/B protocols

- **Analog peripherals**
  - 2 x 12-bit ADCs with a max. sampling rate of 5.25 Msps, supporting 4 internal channels (connected internally to OPAx, measuring VDDH/VBAT, and the internal 1.2 V reference source and TS, etc.) and up to 16 external analog input channels; supporting single-ended and differential input
  - 1 x 12-bit 1 Msps DACs with a buffer
  - Up to 3 operational amplifiers (OPA) supporting single-ended PGA and comparator functions
  - 3 x fast analog comparators (ACMP)
  - Built-in reference voltage sources (VREF) of 1.5/2/2.5/3 V
  - Built-in temperature sensor (TS)

- **Timer**
  - 2 x 16-bit high-performance timers (eQCT™: TIM0/TIM7), each supporting 4 input captures, 3 pairs + 1 PWM output, 3 pairs of dead-time complementary outputs, and break function; supporting PWM precision at 4 times the system clock frequency, up to 1.736 ns (576 MHz @boost mode, system clock 144 MHz), or 2 times the system clock frequency (408 MHz @boost mode, system clock 204 MHz); supporting high-precision input capture HRCAP (576 MHz @boost mode); each timer supports 2 pairs of phase-configurable PWM complementary outputs; the 2 high-performance timers can support a total of 4 pairs of phase-configurable PWM complementary outputs; supporting incremental quadrature encoder and Hall sensor
  - 6 x 16-bit general-purpose timers (TIM1/TIM2/TIM3/TIM4/TIM8/TIM9), each supporting 4 input captures and 4 PWM outputs; supporting PWM precision at 4 times the system clock frequency, up to 1.736 ns (576 MHz @boost mode, system clock 144 MHz), or 2 times the system clock frequency (408 MHz @boost mode, system clock 204 MHz); supporting high-precision input capture HRCAP (576 MHz @boost mode); supporting incremental quadrature encoder and Hall sensor
  - 3 x 16-bit general-purpose timers (TIM14/TIM15/TIM16), each supporting 1 input capture and 2 dead-time complementary PWM outputs, for a total of 3 PWM outputs
  - 1 x 16-bit basic timer (TIM5), able to trigger D/A conversion output
  - 2 x 16-bit low-power timers (LPTIM0/LPTIM1), each supporting 1 input capture and 1 PWM output, for a total of 2 PWM outputs
  - 1 x low-power IWDT, resettable/interruptible
  - 1 x window watchdog timer (WWDT)
  - 1 x 24-bit SysTick timer

- **Real-time clock (RTC)**
  - Hardware perpetual calendar (with seconds, minutes, hours, weekday, date, month and year displayed in BCD format), with calibration supported

- **High-speed interface**
  - 1 USB interface, supporting full-speed USB FS device interface (with integrated PHY)

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- **Hardware acceleration co-processor**
  - Cordic accelerator (supporting sin, cos, arctan, hyperbolic sine, hyperbolic cosine, square root, multiplication, division, etc.)
- **Hardware encryption/decryption engine**
  - Hardware encryption and decryption: supports AES-128/AES-256
  - Random number generator
  - CRC calculation unit
- **Security**
  - Anti-copy board to prevent programs in eFlash from being pirated
  - CRC16-CCITT / CRC32 hardware accelerator
  - Write protection, multiple-read protection
  - External clock stop detection
  - 128-bit UUID
- **Electrical parameters**
  - Operating voltage: 1.8 ~ 3.6 V
  - Operating temperature: -40 ~ 105℃
  - ESD: ± 4 kV (HBM), ± 1.5 kV (CDM)
  - LU：±200 mA@105℃
- **Development support**
  - Built-in Bootloader, supporting UART download, and application updates via ISP and IAP
  - JTAG to SWD mode for online debugging/downloading
  - Complete SDK and EVB HDK
- **Ordering information**

Type	Part No.
256KB Flash	UM32G421-RCT7-0 (LQFP64) UM32G421-RCT7-1 (LQFP64) UM32G421-CCT7 (LQFP48) UM32G421-CCU7 (QFN48) UM32G421-HCU7 (QFN40) UM32G421-KCU7 (QFN32)

Notes:

1. The package of UM32G421-RCT7-0 is LQFP64 (10*10 mm).
2. The package of UM32G421-RCT7-1 is LQFP64 (7*7 mm).

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Contents

1 Product Introduction 1
1.1 Functional Block Diagram 3
1.2 Naming Convention 4
1.3 Configuration Table 5
2 Functional Overview 7
2.1 Core 7
2.2 Hardware Memory Accelerator 7
2.3 Memory 7
2.3.1 Embedded Flash 8
2.3.2 Embedded SRAM 8
2.4 Nested Vectored Interrupt Controller (NVIC) 8
2.5 Clock Architecture 9
2.6 Reset 10
2.7 Power Management Unit (PMU) 10
2.8 Boot Mode 13
2.9 Direct Memory Access Controller (DMA) 13
2.10 DMA Request Multiplexer (DMAMUX) 14
2.11 Universal Asynchronous Receiver Transmitter (UART) 15
2.12 Universal Synchronous / Asynchronous Receiver Transmitter (USART) 17
2.13 Low-power Universal Asynchronous Receiver Transmitter (LPUART) 19
2.14 General-purpose Input/Output (GPIO) 20
2.15 Timer / Counter (TIMx) 20
2.16 Low-power Timer (LPTIM) 22
2.17 Inter-integrated Circuit (I2C) Interface 23
2.18 Real-time Clock (RTC) 24
2.19 Inter-integrated Sound (I2S) Interface 24
2.20 Controller Area Network (CANFD) 25
2.21 Serial Peripheral Interface (SPI) 27
2.22 Independent Watchdog Timer (IWDT) 28
2.23 System Window Watchdog Timer (WWDT) 29
2.24 Hardware Acceleration Co-processor (CORDIC) 29
2.25 Random Number Generator (RNG) 30
2.26 Advanced Encryption and Decryption Algorithm Accelerator (AES) 30
2.27 Universal Serial Bus Full-speed Device Interface (USB) 30
2.28 Analog-to-digital Converter (ADC) 31

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2.29 Digital-to-analog Converter (DAC) 33
2.30 Operational Amplifier (OPA) 33
2.31 Analog Comparator (ACMP) 34
2.32 Temperature Sensor (TS) 34
2.33 Security System 35
2.33.1 UID 35
2.33.2 16/32-bit Hardware CRC Code 35
2.34 Debugging and Programming System 35

3 Pin Definition and Description 37
3.1 Pin Definition 37
3.2 Pin Description 41
3.3 Alternate Function 51

4 Electrical Characteristics 54
4.1 Test Condition 54
4.1.1 Minimum and Maximum Values 54
4.1.2 Typical Value 54
4.1.3 Typical Curve 54
4.1.4 Power Supply Scheme 55
4.2 Absolute Maximum Ratings 55
4.3 Operating Condition 57
4.3.1 General Operating Condition 57
4.3.2 Operating Condition at Power-up / Power-down 58
4.3.3 Embedded Reset and Power Control Block Characteristics 58
4.3.4 Embedded Voltage Reference 59
4.3.5 Supply Current Characteristics 60
4.3.6 External Clock Source Characteristics 65
4.3.7 Internal Clock Source Characteristics 66
4.3.8 Wake-up Time from Low-power Mode 66
4.3.9 PLL Characteristics 67
4.3.10 Flash Memory Characteristics 67
4.3.11 Absolute Maximum Ratings (Electrical Sensitivity) 68
4.3.12 I/O Port Characteristics 69
4.3.13 ADC Electrical Characteristics 70
4.3.14 DAC Electrical Characteristics 71
4.3.15 Operational Amplifier (OPA) Characteristics 72
4.3.16 Analog Comparator (ACMP) Electrical Characteristics 72
4.3.17 Temperature Sensor (TS) Characteristics 73

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5 Package Outline 74
5.1 LQFP64 (10 * 10 mm) 74
5.2 LQFP64 (7 * 7 mm) 75
5.3 LQFP48 (7 * 7 mm) 75
5.4 QFN48 (6 * 6 mm) (Reference) 76
5.5 QFN40 (5 * 5 mm) 76
5.6 QFN32 (4 * 4 mm) 77
6 Revision History 78
7 Contact Us 81

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1 Product Introduction

The UM32G421 series are general microprocessor chips with high performance and low power consumption, based on the ARM® Cortex® -M4 core. The M4 core implements a full set of DSP (digital signal processing) instructions and features a floating-point unit (FPU) and a memory protection unit (MPU). The system clock frequency is up to 204 MHz @ boost mode. The maximum capacity of the built-in Flash is 256 KB, and that of SRAM is 64 KB. They are available at a wide supply voltage of 1.8 V to 3.6 V and in the temperature range from -40 ~ 105℃.

The UM32G421 series chips come with a rich set of peripherals, including:

- 1 x USB FS device interface
- 2 × 12-bit high-speed ADCs
- 1 × 12-bit DAC
- built-in temperature sensor
- 3 × comparators
- 3 × operational amplifiers
- 2 × USARTs
- 4 × UARTs
- 3 × SPIs
- 3 × I2C interfaces
- 1 × I2S interface
- 2 × IWDTs
- 1 × CAN-FD bus interface
- 12 × counters/timers (including advanced control timers and general-purpose timers)
- 2 x LPUARTs

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- 2 × low-power timers
- 1 x 32-bit RTC and counter
- GPIO with up to 54 channels
- integrated hardware Cordic module (supporting sin, cos, arctan, hyperbolic sine, hyperbolic cosine, square root, multiplication, and division)
- built-in encryption/decryption engine (including AES)
- one RNG capable of generating random keys

Applications:

- Motor
- Digital power supply
- General-purpose master control
- IoT applications, etc.

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1.1 Functional Block Diagram

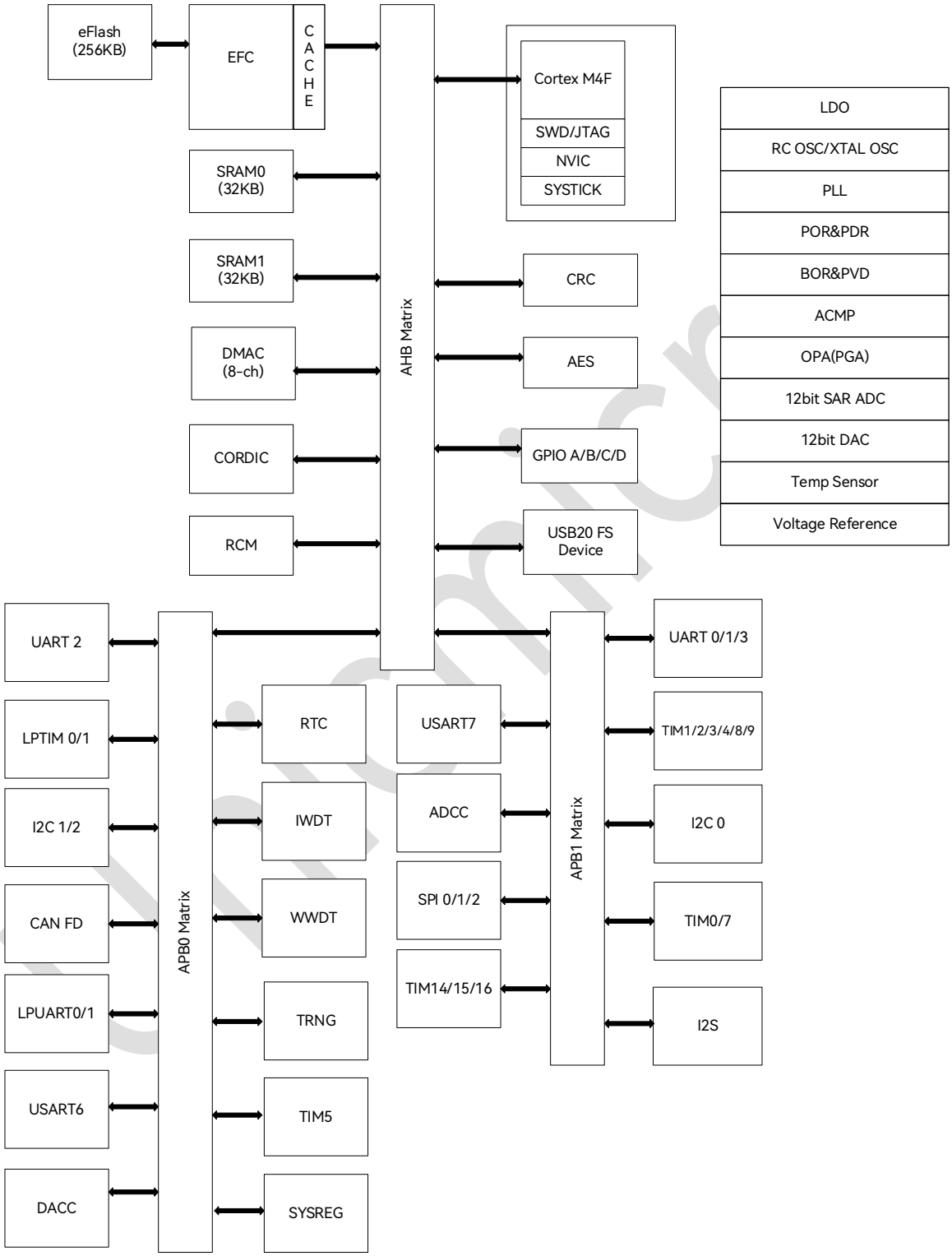

Figure 1-1: Functional Block Diagram

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1.2 Naming Convention

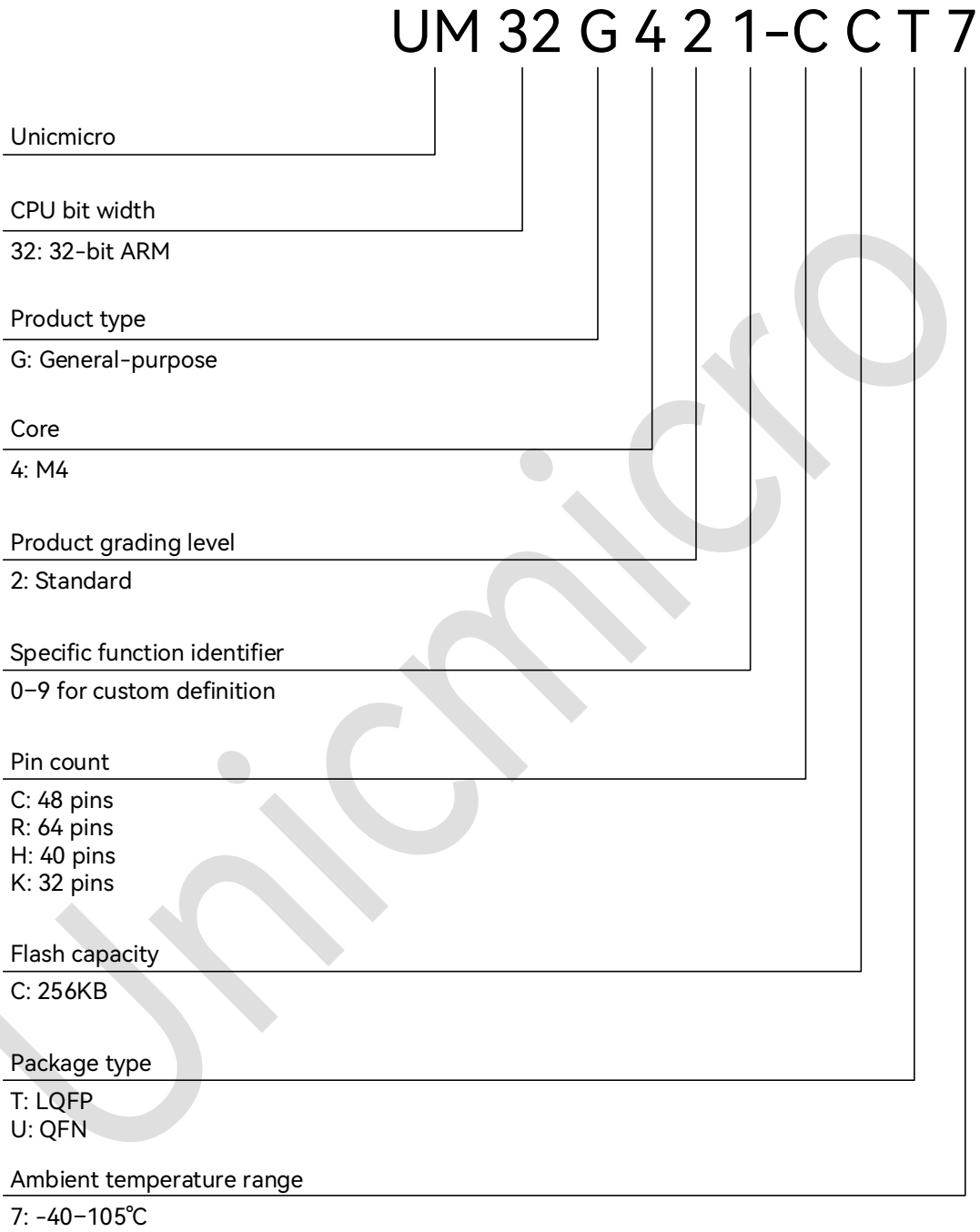

Figure 1-2: Schematic Diagram of Naming Convention

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1.3 Configuration Table

Table 1-1: Configuration Table

Part No.		UM32G421-KCU7	UM32G421-HCU7	UM32G421-CCU7	UM32G421-CCT7	UM32G421-RCT7-1	UM32G421-RCT7-0
Flash (KB)		256					
SRAM (KB)	System	64 (32 + 32)					
	Backup	8 (up to 8KB address space of SRAM1)					
Timer	General-purpose timer	9 (16 bits)					
	Advanced control timer	2 (16 bits)					
	Basic timer	1 (16 bit)					
	SysTick	Yes					
	IWDT	Yes					
	WWDT	Yes					
	LPTIM	2					
Communication interface	SPI	3	3	3	3	3	3
	I2S	1					
	I2C	3					
	USART	2					
	UART	4	4	4	4	4	4
	LPUART	2					
	CANFD	1					

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Part No.		UM32G421-KCU7	UM32G421-HCU7	UM32G421-CCU7	UM32G421-CCT7	UM32G421-RCT7-1	UM32G421-RCT7-0
	USB FS device	No	1	1	1	1	1
	PWM channels	23	26	30	30	37	37
RTC		No	No	1	1	1	1
GPIO		29	36	43	40	54	51
DMA Channels		1 8					
Analog	12-bit ADC Channels	2 13	2 15	2 16	2 12	2 16	2 16
	12-bit DAC Channels	1 1					
	Internal voltage reference	No	Yes	Yes	Yes	Yes	Yes
	OPA (PGA)	3					
	ACMP	3					
	TS	Yes					
CORDIC algorithm module		Yes					
Hardware encryption/decryption engine	CRC	Yes					
	AES (256)	Yes					
	RNG	Yes					
Powered by $V_{battery}$		No	No	No	Yes	Yes	Yes
Maximum CPU frequency		204 MHz @ boost mode					
Operating voltage		1.8 ~3.6 V					
Operating temperature		Ambient temperature: -40 ~ +105℃					
Package		QFN32 (4 * 4 mm)	QFN40 (5 * 5 mm)	QFN48 (6 * 6 mm)	LQFP48 (7 * 7 mm)	LQFP64 (7 * 7 mm)	LQFP64 (10 * 10 mm)

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2 Functional Overview

2.1 Core

The ARM® Cortex®-M4F processor, the latest generation of embedded processors, is developed based on the Cortex®-M3 core, with strengthened computational capabilities, newly-added FPU, DSP and parallel computing instructions, delivering superior performance of 1.25 DMIPS/MHz. The combination of its efficient signal processing capabilities with the low power consumption, low cost, and ease of use of the Cortex-M series processors makes it ideal for applications requiring a mix of control and signal processing capabilities that are easy to use.

The ARM® Cortex®-M4F is a 32-bit RISC processor with outstanding code efficiency.

2.2 Hardware Memory Accelerator

The memory accelerator optimized for the industrial-standard ARM® Cortex®-M4F is provided with a 2KB instruction cache. It balances the inherent performance advantage of the ARM® Cortex™-M4F over the traditional Flash memory technologies, which requires the processor to wait for the Flash memory at higher operating frequencies. Based on Core-Mark benchmark, the performance achieved thanks to this accelerator is equivalent to 0-wait-state program execution from Flash memory at a CPU frequency of up to 204 MHz.

2.3 Memory

The chip integrates embedded Flash and embedded SRAM.

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2.3.1 Embedded Flash

It embeds a 256KB eFlash for storing programs and data. The page size is 4K bytes, and it supports operations such as full-chip erase, page erase, read, and write.

2.3.2 Embedded SRAM

Main features:

- System SRAM up to 64 KB, including 32KB SRAM0 and 32KB SRAM1, and it can be accessed by CPU without wait state.
- 8KB backup SRAM (up to 8KB address space of SRAM1)

2.4 Nested Vectored Interrupt Controller (NVIC)

The nested vectored interrupt controller is able to handle multiple maskable interrupt channels (not including the 16 Cortex®-M4F interrupt lines) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt vector entry address passed directly to the core
- Closely coupled NVIC interface
- Allowing early processing of interrupts
- Processing of late-arriving higher-priority interrupts
- Supporting interrupt tail chaining
- Processor state automatically saved
- Interrupt priority levels restored on interrupt exit with no instruction overhead

The NVIC hardware module provides flexible interrupt management with minimal interrupt latency.

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2.5 Clock Architecture

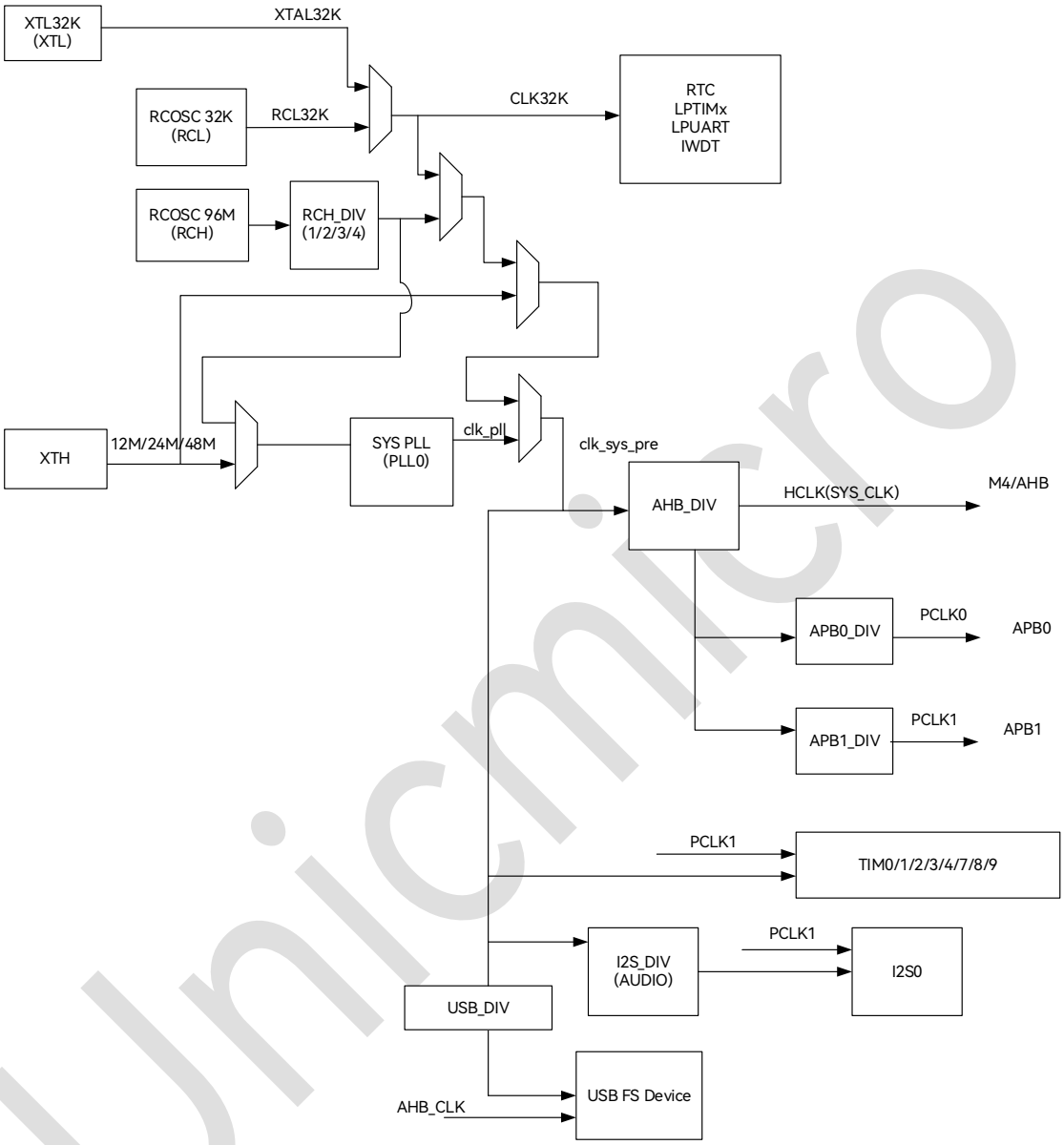

Figure 2-1: Clock Architecture Diagram

Four different sources can deliver the system clock:

- High-precision internal RCH of 96 MHz
- Internal RCL of 32 kHz
- External crystal XTL of 32.768 kHz
- External crystal XTH

There is an internal PLL for system, audio and USB clocks.

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The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It features a 96 MHz internal RC oscillator (RCH), an external high-speed crystal oscillator (XTH), a 32 kHz internal RC oscillator (RCL), an external low-speed crystal oscillator (XTL), a PLL, an XTH monitor, clock prescaler, clock multiplexer and clock gating circuitry.

AHB, APB and Cortex™-M4 are derived from the system clock (SYS_CLK), and the clock source of SYS_CLK can be XTH, RCH, PLL, or RCL/XTL with a low frequency of 32 kHz. The IWDT and the RTC are derived from a low-frequency clock source (RCL or XTL).

2.6 Reset

The reset modes are shown in the following table:

Table 2-1: Reset Mode

Reset Mode	Trigger Condition
Power-on and power-down reset (POR & PDR)	Power-on and power-down of V_{DDH} (1.8–3.6 V) and power-on of internal core voltage
RESETN pin reset	Low-level input on the external RESETN pin
Brownout reset (BOR)	V_{DDH} drops below the V_{BOR} threshold
Low voltage detection reset (LVD)	V_{DDH} drops below the V_{LVD} threshold
Window watchdog reset (WWDT)	-
Independent watchdog reset (IWDT)	-
Software reset	-
External high-speed oscillator failure reset	Reset triggered when the external high-speed oscillator stops abnormally

2.7 Power Management Unit (PMU)

The chip supports single power supply and VBAT backup power supply. It requires an external operating supply voltage between 1.8 V and 3.6 V, and a digital circuit operating voltage generated by the built-in LDO.

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VDDH: 1.8 ~ 3.6 V, the VDDH pin supplies power to the I/O, the internal regulator and some analog IPs.

VDDA: 1.8 ~ 3.6 V, the VDDA pin supplies power to analog IPs such as ADC/DAC.

VBAT: 1.8 ~ 3.6 V, the VBAT pin supplies power to always-on modules such as BKSRAM and RTC in Standby mode.

It also supports multiple low-power modes: sleep mode, stop mode, standby mode, and deep standby mode.

Table 2-2: Low-power Modes Summary

Power Mode	Descriptions	Entry Condition	Wakeup Source
Run mode	All supplies are powered on, and the high-speed clock remains active.	-	-
Sleep mode	All supplies are powered on, with the M4 core high-speed clock off and other peripherals on.	1. PMU_STANDBY_EN = 0, PMU_MODE[1:0] = 00, PMU_BKSRAMOFF = 0 2. EFC_Sys_Mode = 0 3. WFI/WFE	1. Wake-up by any GPIO interrupt 2. Wake-up by any peripheral interrupt 3. Wake-up by reset (RESETN, IWDT reset)
Stop mode	All supplies are powered on, with high-speed clock off and 32 kHz low-speed clock on.	1. PMU_STANDBY_EN = 0, PMU_MODE[1:0] = 01, PMU_BKSRAMOFF = 0 2. EFC_Sys_Mode = 0 3. Set SLEEPDEEP = 1 for M4 core. 4. WFI/WFE	1. Wake-up by any GPIO interrupt 2. Wake-up by RTC alarm interrupt, RTC timestamp and tamper interrupts 3. Wake-up by IWDT reset or interrupt 4. Wake-up by external LPUART 5. Wake-up by LPTIM0–1 timing

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Power Mode	Descriptions	Entry Condition	Wakeup Source
Standby0 mode	The CORE domain is powered off, the BBU domain is kept on, and the 32 K low-speed clock remains active. BKSRAM / IWDT / LPTIM / LPUART are powered on.	1. PMU_STANDBY_EN = 1, PMU_MODE[1:0] = 10, PMU_BKSRAMOFF = 0 2. EFC_Sys_Mode = 1 3. Set SLEEPDEEP = 1 for M4 core. 4. WFI/WFE	1. Wake-up by external pins PA0, PA2, PC0, PC2, PC3 and PC13 2. Wake-up by RTC alarm interrupt, RTC timestamp and tamper interrupts 3. Wake-up by LPTIM0–1 timing 4. Wake-up by LPUART (only PC2) 5. Wake-up by IWDT reset or interrupt 6. Wake-up by reset (RESETN)
Standby1 mode	The CORE domain is powered off, the BBU domain is kept on, and the 32 K low-speed clock remains active. BKSRAM / IWDT / LPTIM / LPUART are powered off.	1. PMU_STANDBY_EN = 1, PMU_MODE[1:0] = 10, PMU_BKSRAMOFF = 1 2. EFC_Sys_Mode = 1 3. Set SLEEPDEEP = 1 for M4 core. 4. WFI/WFE	1. Wake-up by external pins of PA0, PA2, PC0, PC2, PC3 and PC13 2. Wake-up by RTC alarm interrupt, RTC timestamp and tamper interrupts 3. Wake-up by reset (RESETN)
DeepStandby0 mode	The CORE domain is powered off, the BBU domain is kept on, and the 32 K low-speed clock is inactive. BKSRAM / IWDT / LPTIM / LPUART are powered on.	1. PMU_STANDBY_EN = 1, PMU_MODE[1:0] = 11, PMU_BKSRAMOFF = 0 2. EFC_Sys_Mode = 1 3. Set SLEEPDEEP = 1 for M4 core. 4. WFI/WFE	1. Wake-up by external pins of PA0, PA2, PC0, PC2, PC3 and PC13 2. Wake-up by reset (RESETN)
DeepStandby1 mode	The CORE domain is powered off, the BBU domain is kept on, and the 32 K	1. PMU_STANDBY_EN = 1, PMU_MODE[1:0] = 11, PMU_BKSRAMOFF = 1 2. EFC_Sys_Mode = 1	1. Wake-up by external pins of PA0, PA2, PC0, PC2, PC3 and PC13 2. Wake-up by reset

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Power Mode	Descriptions	Entry Condition	Wakeup Source
	low-speed clock is inactive. BKSRAM / IWDT / LPTIM / LPUART are powered off.	3. Set SLEEPDEEP = 1 for M4 core. 4. WFI/WFE	(RESETN)
Power-off mode	All supplies are powered off.	Powering off external V_{DDH} & V_{BAT}	Power on

Notes:

- The BBU domain includes RTC, backup register and PMU logic.
- In standby mode, I/O status hold is optional. In wakeup status, the I/O pins return to the power-on reset state (most of the I/O pins return to the high resistance).

2.8 Boot Mode

The system executes from address 0x0000_0000 upon power-on of the chip.

Table 2-3: Boot Mode

BOOT1 (PB2)	BOOT0	Boot
x	0	Boot from main flash
0	1	Boot from system memory
1	1	Boot from SRAM

Note: It meanwhile supports writing specific NVR addresses, and directly boots from main flash upon power-up.

2.9 Direct Memory Access Controller (DMA)

The DMA is used to provide high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions, which keeps the CPU resources free for other operations, thus improving the system efficiency.

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The chip embeds one DMA controller (DMA0) that supports a total of 8 channels.

Main features:

- Cancontrol data transfer among multiple modules
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral data transfers
- Each controller is provided with 8 DMA channels.
- Configurable bit width and block length of data transfer
- Channel 0 & 1 with 4 x 32-bit FIFOs, channels 2 ~ 7 with 2 x 32-bit FIFOs
- Block length up to 4095
- Multi-block operations
- Reload operation
- Supporting fixed and incremental source address transfers
- Supporting fixed and incremental destination address transfers

2.10 DMA Request Multiplexer (DMAMUX)

The chip embeds one DMAMUX module, which can be freely mapped to the 8 handshake signals of the DMA controller, and then matched to the 8 channels of the DMA controller.

Main features:

- Up to 8-channel programmable DMA request line multiplexer output
- Up to 4-channel DMA request generator
- Up to 8 trigger inputs for DMA request generator
- Up to 16 synchronization inputs
- Each DMA request generator channel includes:
  - DMA request trigger input selector

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- DMA request counter
- Event overflow flag of the selected DMA request triggers input

- Each DMA request line multiplexer channel output has:
  - Up to 79 input DMA request lines from peripherals
  - One DMA request line output
  - Synchronization input selector
  - DMA request counter
  - Event overflow flag of the selected synchronization input
  - One event output for DMA request link

2.11 Universal Asynchronous Receiver Transmitter (UART)

UART is a widely used serial communication interface that supports full-duplex communication. The UART converts parallel data from memory or a processor into serial data for transmission to an external UART receiver, or it converts serial data received from an external UART device into parallel data for the processor. UART supports serial communication with external interface devices.

Wherein, UART1 is an enhanced serial port, while UART0, UART2 and UART3 are basic general-purpose serial port modules.

UART1 main features:

- 16-byte hardware FIFO
- Baud rate supports both integer and fractional division
- CTS/RTS flow control
- Error start bit detection

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- Frame interrupt detection
- Circuit-break detection
- Setting of data bit width (5–9 bits) and number of stop bits (1 bit, 1.5 bits and 2 bits)
- Fixed parity, even/odd parity or no parity for data
- IrDA 1.0 protocol with baud rate ranging from 9.6 k to 115.2 k
- DMA operation

UART0/UART2/UART3 main features:

- Providing standard asynchronous communication data formats
  - Generating a 1-bit start bit
  - Generating a 1-bit parity bit (odd or even configurable) or no parity bit
  - Generating a 1-bit stop bit
- Bytes transmitted sequentially from LSB to MSB
- 8-bit 4-level RX FIFO
- Programmable baud rate (adjustable based on the frequency divider parameters)
- Supporting data communication and error handling interrupt
- Status bit can be accessed by either polling or interrupt
- Providing FIFO non-empty, half-full, full, and overflow flags
- Flags of transmit data errors and parity errors
- Supporting transmission at common baud rates such as 9600 bps, 19200 bps and 115200 bps
- Self-test mode, i.e., receiving the data transmitted by itself

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2.12 Universal Synchronous / Asynchronous Receiver Transmitter (USART)

USART provides a complete full-duplex universal synchronous / asynchronous serial link. To ensure the highest standard, the data frame format can be programmed in a wide range (data length, parity, number of stop bits, etc.) This receiver implements detection of parity error, frame error and overflow error. Receiver timeout allows handling of frames with variable lengths, and transmitter time protection facilitates communication with slow remote devices. Multiprocessor communication can also be supported by address bit processing in reception and transmission.

Main features:

- Programmable baud rate generator
- 5-bit to 9-bit full-duplex synchronous or asynchronous serial communication
  - 1, 1.5 or 2 stop bits in asynchronous mode; or 1 or 2 stop bits in synchronous mode
  - Parity generation and error detection
  - Frame error detection and overflow error detection
  - MSB first or LSB first for data transfer
  - Optional open-circuit mark generation and detection
  - Receiver sampling rate of 8 or 16 times the baud rate
  - Receiver timeout and transmitter time protection
  - Multipoint mode with address generation and detection
- IrDA modulation/demodulation
  - Communication rate up to 115.2 kbps
- SPI mode

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- Master or slave
- Programmable serial clock phase and polarity
- SPI serial clock (SCK) frequency up to MCK/2 of the internal clock frequency

- LIN mode
  - Complying with LIN1.3 and LIN2.0 specifications
  - Master or slave
  - Handling frames of up to 256 data bytes
  - Response data length configurable or automatically defined by the identifier
  - Self-synchronization in slave node configuration
  - Automatic processing and verification of “Synch Break” and “Synch Field”
  - Detection of “Synch Break” even if it is partially overlapped with a data byte
  - Automatic identifier parity calculation, transmission and verification
  - Parity transmission and verification can be disabled
  - Automatic checksum calculation, transmission and verification
  - Checksum transmission and verification can be disabled
  - Supporting both “Classic” and “Enhanced” checksum types
  - Complete LIN error checking and reporting
- DMA operation

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2.13 Low-power Universal Asynchronous Receiver Transmitter (LPUART)

LPUART is a low-power UART that supports data reception at a maximum baud rate of 9600 bps when operating at 32 kHz clock, and a maximum baud rate of 115200 bps when operating at APB0 clock.

Main features:

- Asynchronous data transmission and reception
- Standard UART frame format
  - 1 start bit
  - 7 or 8 data bits
  - Odd parity, even parity or no parity bit
  - 1 or 2 stop bits
- Operating with a 32768 Hz XTL clock or a 32 kHz RCL clock, supporting baud rates from 300 to 9600 bps
- Baud rate reaching up to 115200 bps when using the APB0 clock (PCLK0 clock source)
- Programmable data polarity
- Interrupt flags
  - Receive buffer full flag
  - Receive buffer overflow flag
  - Receive frame format error flag
  - Receive parity bit error flag
  - Start detection flag
  - Data matching flag

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  - Transmission complete flag
- Wake-up in low-power mode
  - Wake-up on RXD falling edge interrupt
  - Wake-up on start bit detection
  - Wake-up on completion of receiving 1 byte
  - Wake-up on matching 1 byte of data
- An external low-speed clock must be used for meeting the clock accuracy.

2.14 General-purpose Input/Output (GPIO)

Up to 54 GPIOs are available. Each port is controlled by an independent control register bit. They support edge-triggered interrupts and level-triggered interrupts to wake up the chip from various low-power modes to run mode. They are integrated with pull-up and pull-down resistors with Schmitt trigger input filtering function. The output drive capability is configurable, with a maximum current drive capability of 20 mA. The 54 GPIOs support external asynchronous interrupts, wherein, 28 GPIOs can support 5 V withstand voltage input.

2.15 Timer / Counter (TIMx)

5 x 16-bit high-performance timers (eQCT™: TIM0 / TIM7), each timer supports 4 input captures, 3 pairs +1 PWM output, 3 pairs of dead-time complementary outputs, the break function, the two-phase hardware phase shift function, PWM precision with 4x system clock frequency (up to 576 MHz @ boost mode, system clock 144 MHz), and high-precision input capture HRCAP with 4x system clock frequency (576 MHz @ boost mode, system clock 144 MHz). Each timer supports 2 pairs of phase-configurable PWM complementary outputs (CH1/CH1N and CH3/CH3N, or CH2/CH2N and CH3/CH3N). In total, the two high-

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performance timers can support 4 pairs of phase-configurable PWM complementary outputs, and support incremental quadrature encoder and Hall sensor.

6 x 16-bit general-purpose timers (TIM1/TIM2/TIM3/TIM4/TIM8/TIM9), each timer supports 4 input captures and 4 PWM outputs, PWM precision with 4x system clock frequency (up to 576 MHz @ boost mode, system clock 144 MHz), high-precision input capture HRCAP with 4x system clock frequency (576 MHz @ boost mode, system clock 144MHz), and incremental quadrature encoder and Hall sensor.

5 x 16-bit general-purpose timers (TIM14/TIM15/TIM16), each with 1 input capture and 1 pair of complementary PWM outputs with dead-time insertion.

1 x 16-bit basic timer (TIM5), able to trigger DAC output.

The timer functions are compared as follows:

Table 2-4: Timer Function Comparison

Timer Type	Timer	Resolution	Type	Prescaler Factor	DMA Request Generation	Capture / Compare Channels	Complementary Output
Advanced timer	TIM0 TIM7	16	Up, down, up/down	Any integer between 1 and 65536	Y	4	Y
General timer	TIM1 TIM2 TIM3 TIM4 TIM8 TIM9	16	Up, down, up/down	Any integer between 1 and 65536	Y	4	N
General timer	TIM14 TIM15 TIM16	16	Up, down, up/down	Any integer between 1 and 65536	Y	1	Y

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Timer Type	Timer	Resolution	Type	Prescaler Factor	DMA Request Generation	Capture / Compare Channels	Complementary Output
Basic timer	TIM5	16	Up	Any integer between 1 and 65536	Y	0	N
Low-power timer	LPTIM0 LPTIM1	16	Up	Any integer between 1 and 65536	N	1	N

2.16 Low-power Timer (LPTIM)

LPTIM is a 16-bit low-power timer/counter module running in always-on power domain. By selecting suitable clock source, LPTIM is able to keep running in various low-power modes with extremely low power consumption. LPTIM can be used as an external pulse counter in low-power mode even with no internal clock source. Also, in combination with an external input trigger signal, LPTIM is able to realize timeout wake-up from low-power modes.

Main features:

- 16-bit up counter
- 3-bit asynchronous prescaler with 8 possible dividing factors (1, 2, 4, 8, 16, 32, 64, 128)
- Selectable clock sources:
  - Internal clock sources: LSCLK (XTL or RCL), CLK1Hz, APB0 (PCLK0)
  - External clock source: LPTIMx_IN
- 16-bit compare register

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- 16-bit target register
- Software/hardware trigger
- Configurable input polarity
- External pulse counting with no clock source
- Externally triggered timeout wake-up from low-power modes
- 16-bit PWM

2.17 Inter-integrated Circuit (I2C) Interface

I2C interface supports master / slave mode. Wherein I2C0 is standard I2C interface, while I2C1/I2C2 are enhanced I2C interfaces.

I2C0 main features:

- Master receive/transmit, slave receive/transmit
- Standard mode (100 Kb/s) / fast mode (400 Kb/s) / fast mode+ (1 Mb/s)
- 7-bit and 10-bit addressing
- Broadcast addressing
- Up to 4 slave addresses
- Interrupt polling

I2C1 / I2C2 main features:

- Master receive/transmit, slave receive/transmit
- Up to 1 Mbps operating rate

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- 7-bit and 10-bit addressing mode
- Interrupt polling
- RX FIFO and TX FIFO with a depth of 2 bytes each
- DMA acceleration

2.18 Real-time Clock (RTC)

The RTC supports calendar with subsecond, seconds, minutes, hours, week day, date, month and year displayed in BCD (binary-coded decimal) format; and also supports an alarm, a periodic wake-up source, a tamper detector and an 80-byte backup register.

2.19 Inter-integrated Sound (I2S) Interface

The inter-IC sound bus (I2S) is a standardized communication interface developed by Philips for use in many (super) large-scale IC-based systems, especially in many digital stereo audio systems.

Main features:

- Master and slave modes
- Simplex transmitting, simplex receiving, duplex transceiving
- Philips standard, left-justified and right-justified standards, PCM (with short and long frame) standard
- Configurable audio channel length: 16 or 32 bits
- Configurable audio data length: 8, 16, 24 or 32 bits

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- Stereo / mono audio data available in non-PCM mode
- The stereo audio data can be transmitted first via left channel or first via right channel.
- The mono audio data can be transmitted via left channel or right channel.
- In non-PCM mode, the polarity of WS is optional.
- In non-PCM mode, the moment of switching between SD and WS is optional on the rising or falling edge of SCK; while in PCM mode, it is fixed on the rising edge of SCK.
- Built-in 8-word TX FIFO and RX FIFO (1 word = 32 bits), each can store 16 pieces of 16-bit data or 8 pieces of 32-bit data.
- MCLK generated by PLL is required when audio block is defined as Master at 256 times the audio sampling rate (Fs), which is typically 8 / 11.025 / 16 / 22.05 / 24 / 32 / 44.1 / 48 / 96 / 192 kHz.
- If interrupt is enabled, the following conditions will trigger an interrupt:
  - TX FIFO with enough space
  - RX FIFO with enough data
  - TX FIFO under-load
  - RX FIFO overflow
- DMA operation

2.20 Controller Area Network (CANFD)

The CAN controller, with a maximum data rate of 8 Mbps, being compliant with CANFD and CAN2.0 A/B protocols, can be used in the fields of automotive electronics and industrial control.

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Main features:

- Complying with ISO 11898-1:2015 specification
- Supporting CAN and CAN FD formats
- Up to 64 bytes data frame
- Flexible data rates
- Data transmission rate up to 5 Mbps
- Hardware data filter (single / double-filter optional)
- Supporting transmission and reception via DMA
- 3 transmit buffers
- 256-byte RX FIFO and 256-byte TX FIFO
- Over-load frame generated at FIFO overflow
- Protocol exception event detection
- Normal mode and listening mode
- Up to 32 configurable receive filters
- Transmitter delay compensation, with the length of up to three data bits
- Single transmission
- Transmission can be aborted
- Error counter readable

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2.21 Serial Peripheral Interface (SPI)

The synchronous serial interface supports both master and slave modes. It also supports DMA hardware data transfer.

SPI is widely used to provide an economical board-level interface between different devices such as EEPROM, FLASH, Micro Controller, DAC, ADC, etc

SPI0/SPI1 are basic SPI interfaces. SPI2 is an enhanced SPI interface.

SPI0/ SPI1 main features:

- Full-duplex 4 wires or half-duplex 3 wires serial synchronous transmission and reception
- Master/slave mode
- Programmable clock polarity and phase
- Programmable bit rate
- Up to f_{sys} / 2 frequency in slave mode
- Transmission complete interrupt flag
- Write conflict error flag
- Error detection, protection and interrupt flags in master mode
- Built-in 8-byte FIFO
- DMA single word transmission
- Supporting 2 slave devices

SPI2 main features:

- Configurable master or slave mode

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- Supporting serial full duplex, half duplex, simplex transmitting and simplex receiving in both master and slave modes
- Configurable 16-bit SPI clock frequency control register: SCK frequency up to $f_{PCLK}/2$ in master mode while up to $f_{PCLK}/4$ in slave mode
- Programmable SCK polarity and phase
- Supporting SPI Motorola mode or TI mode
- Programmable data order with MSB-first or LSB-first shifting
- Configurable character length from 4 bits to 32 bits, defaulting to 8 bits
- 8-level 32-bit wide TX FIFO and RX FIFO
- Programmable software- or hardware-controlled chip select
- DMA operation

2.22 Independent Watchdog Timer (IWDT)

The watchdog timer can generate a non-maskable interrupt or reset when the counter reaches the given timeout value. It can be used to regain control when the system fails to respond as expected due to software errors or external device failures.

Main features:

- 32-bit downcounter with programmable load
- Independent watchdog timer enabled
- Interrupt generation logic with interrupt masking
- Lockout register for software runaway protection

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- Software boot function: reset enabling / disabling in WDT control register
- The register configuration of timer counting can be suspended when the CPU is suspended during debugging.

2.23 System Window Watchdog Timer (WWDT)

The system window watchdog is a watchdog running synchronously with CPU, aiming at monitoring the running status of CPU in real time, so that it can reset CPU in the case of abnormal operation to avoid unpredictable consequences.

To ensure synchronization and real-time performance, the WWDT operates using the PCLK clock, with an internal prescaler circuit to generate a synchronous counting enable signal.

Main features:

- In up-counting mode, the counter counts from 0 to the overflow time.
- The window period is 50% of the counter time greater than or equal to the overflow time.
- With early warning interrupt function, which triggers an interrupt at 75% of the overflow time.

2.24 Hardware Acceleration Co-processor (CORDIC)

The CORDIC controller can use the CORDIC algorithm to calculate functions such as $m \cdot \sin\theta$, $m \cdot \cos\theta$, $\mathrm{atan2(y,x)}$, $\sqrt{x^2+y^2}$, $y \cdot x$, $\mathrm{y/x}$, $\sinh w$, $\cosh w$, $\tanh^{-1}(y/x)$, $\ln x$, $\sqrt{\mathrm{x}}$, etc.

Main features:

- 24-bit precision calculation
- AHB interface supporting input and output of 16-bit and 32-bit data

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2.25 Random Number Generator (RNG)

The RNG is capable of delivering random numbers. RNG is capable of delivering random numbers from random seeds.

2.26 Advanced Encryption and Decryption Algorithm Accelerator (AES)

The AES module encrypts or decrypts data using AES-128 or AES-256 algorithm defined in Federal information processing standards (FIPS) publication 197.

Main features:

- Cipher key lengths of 128 or 256 bits
- AES encryption and decryption
- Electronic code book (ECB) and cipher block chaining (CBC) modes
- SWAP mode supported for data input and output, i.e., big-endian / little-endian format configurable
- Hardware MASK supported during encryption and decryption

2.27 Universal Serial Bus Full-speed Device Interface (USB)

The USB device controller is a device interface compatible with the USB 2.0 full-speed protocol. It is used in conjunction with the USB PHY to support communication between the chip and the USB HOST.

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Main features:

- Compatible with USB1.1 and USB2.0 full-speed protocols
- 4 general-purpose bidirectional transfer endpoints (EP1, EP2, EP3, EP4)
- Endpoints support a maximum packet length of 64 bytes, and support both memory and FIFO accesses
- FIFO mode supports 32-bit access
- Memory access mode: 8-bit, 16-bit, 32-bit
- Suspend, resume and remote wake-up functions
- Hardware toggle comparison and software control functions
- Interrupt generation for data transfer on each endpoint
- Interrupt enabled for bus reset, suspend and resume
- Optional CRC error reply with NAK
- Automatic reply with NAK for data packets exceeding the maximum packet length (64 bytes)
- USB device reply with NAK for the next IN operation if the host does not reply with ACK for the IN operation
- Supporting detection of lost EOP in token packets and data packets, and optional automatic NAK response for lost EOP

2.28 Analog-to-digital Converter (ADC)

The device embeds two 12-bit SAR ADCs with a sampling rate up to 5.25 Msps, supporting single-ended input and differential input. It can measure 16 external channels and 4 internal

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channels (supporting internal OPA measurement, internal 1.2 V reference source, VDDH measurement and VBAT measurement).

Main features:

- 12-bit successive approximation ADC
- ADC supply: 1.8–3.6 V, ADC input range: $V_{REF-} \leq V_{IN} \leq V_{REF+}$
- V_{REF} optional reference: V_{DDA}, internal reference voltage V_{REF} of 1.5/2.0/2.5/3 V, or external input V_{REF}
- The two ADCs can be used in conjunction with the internal operational amplifier (OPA) to amplify the signal before sampling or as a buffer.
- Trigger mode: triggered by software configuration register, or internal timer event (rising edge, falling edge or both edges), or GPIOA interrupt
- Conversion modes: single-shot mode, continuous mode, discontinuous mode, dual-ADC cooperative mode
- Regular and injection sequences: A regular group is composed of up to 16 channel conversions, and an injected group is composed of up to 4 channel conversions. Both groups consist of a sequence of conversions that can be done on any channel and in any order. The injection sequence has higher priority over the regular sequence.
- It is able to continuously handle multiple times (2, 4, 8, 16, 32, 64 or 128 times) sampling conversions on one or some channels and calculate the average.
- It is provided with an analog watchdog for monitoring the conversion result.
- Each channel has an independent data register, which can be uniformly set to clear data automatically after reading.

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- Each of the ADCs is provided with a 32-level deep and 16-bit wide RX FIFO for storing the conversion results of the regular and injection conversions.
- Supporting DMA operation
- In-chip temperature measurement with temperature sensor (TS)
- Measuring VBAT battery level
- Measuring external power supply VDDH
- Measuring internal 1.2 V reference source

2.29 Digital-to-analog Converter (DAC)

The built-in independent DAC module can be used to convert 12-bit digital signals into analog voltage signal outputs.

Main features:

- 8-bit or 12-bit digital input
- Simultaneous update of conversion data for two converters
- Generation of triangular waves and noise waves
- DMA operation
- External trigger to update conversion data

2.30 Operational Amplifier (OPA)

Main features:

- Supporting OPA function

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- Supporting single-ended PGA function with gain options of 1/2/4/8/16/32/64x (using internal feedback resistors), and PGA function with variable gain x (using external feedback resistors)
- Can be used as an analog comparator
- Can be used as a buffer to cooperate with ADC

2.31 Analog Comparator (ACMP)

The ACMP module is used to compare the magnitudes of two input analog voltages and output a high or low level based on the comparison result. When the voltage at the “INP” input pin is higher than that at the “INM” input pin, the comparator outputs a high level; when the voltage at the “INP” input pin is lower than that at the “INM” input pin, the comparator outputs a low level.

Main features:

- The analog comparator output can generate an interrupt.
- The comparator output can be used as a TIMx break input or output to an external pin.
- Typical 100 ns

2.32 Temperature Sensor (TS)

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature. It is internally connected to the ADC input channel which is used to convert the sensor output voltage into a digital value.

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2.33 Security System

2.33.1 UID

Each chip is shipped with a 16-byte unique device identifier, including wafer lot information, chip coordinate information, etc.

2.33.2 16/32-bit Hardware CRC Code

The CRC controller can perform CRC calculation using various polynomials.

Main features:

- Supporting the following polynomials:
  - $x^{16} + x^{12} + x^5 + 1$
  - $x^{16} + x^{15} + x^2 + 1$
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x^1 + 1$
- Input data types: byte, half-word, word
- The input data can be reversed by bit, half-word, byte, initial value and result value.

2.34 Debugging and Programming System

The debugging and programming system features are as follows:

- **Embedded debugging system**

  The embedded debugging solution provides a full-featured real-time debugger with standard and mature debugging development software such as Keil / IAR, supporting 4

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hardware breakpoints and multiple soft breakpoints.

- **Online programming mode**

  Online programming is supported, and several milliseconds after reset is in ISP mode, followed by user mode.

- **High security**

  The encrypted embedded debugging solution provides a full-featured real-time debugger.

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3 Pin Definition and Description

3.1 Pin Definition

The UM32G421 comes in a variety of packages. The pin function is configured by IO control register, and all pins except the power pin and the RESETN pin are configured with alternate functions. After system reset, the pin function will be set to the default value.

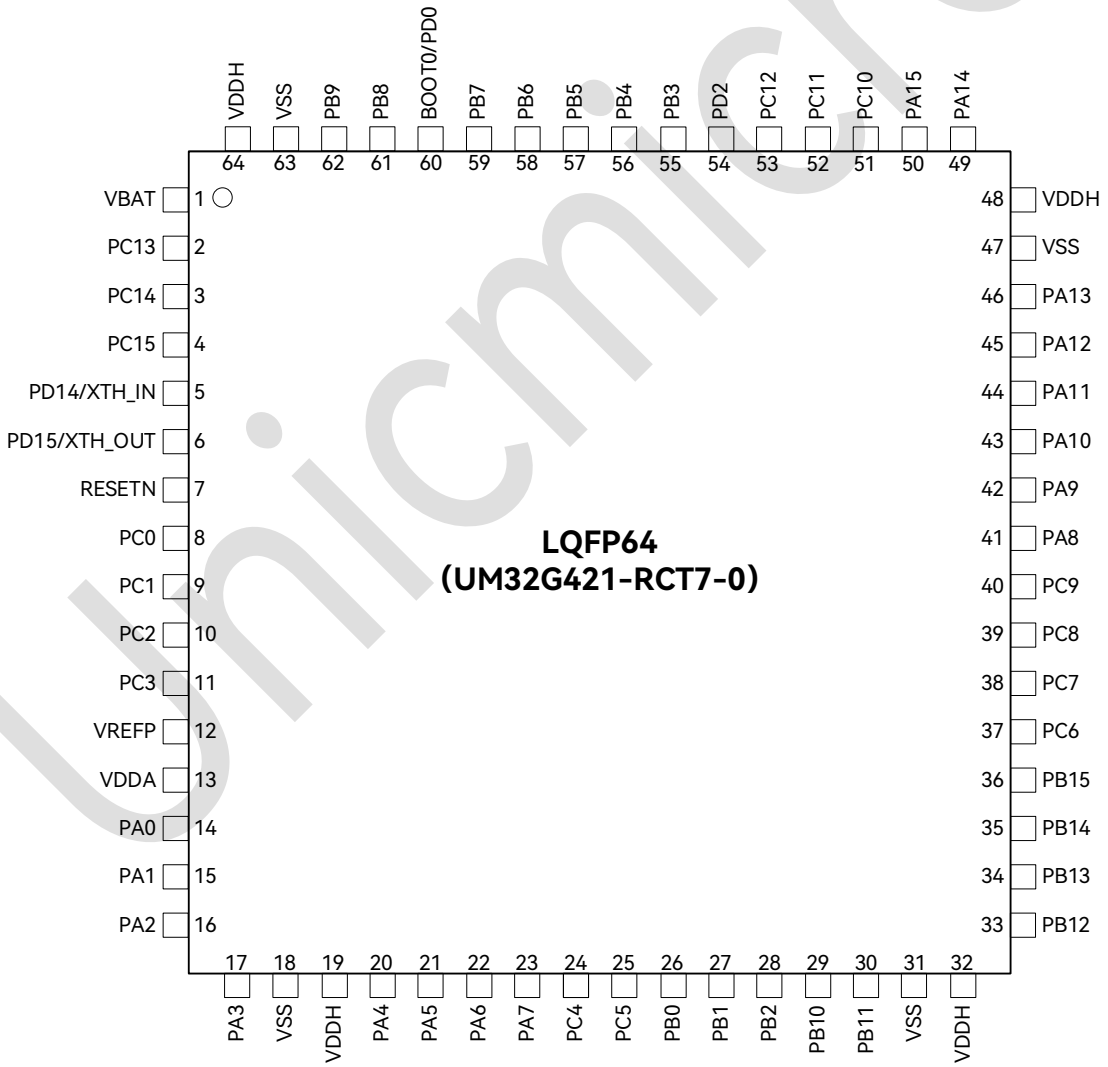

Figure 3-1: LQFP64 (10 * 10 mm) Pinout Diagram

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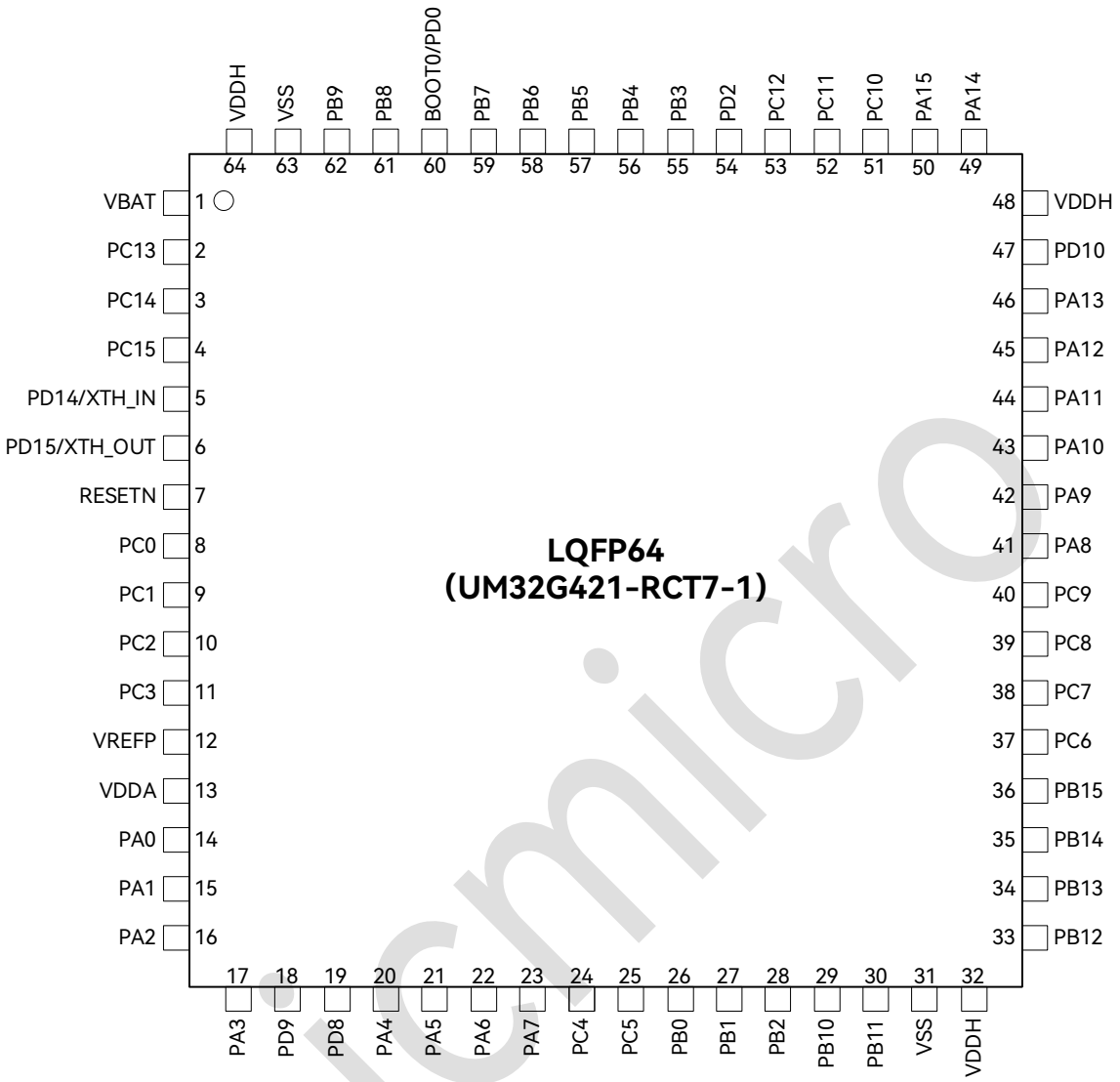

Figure 3-2: LQFP64 (7 * 7 mm) Pinout Diagram

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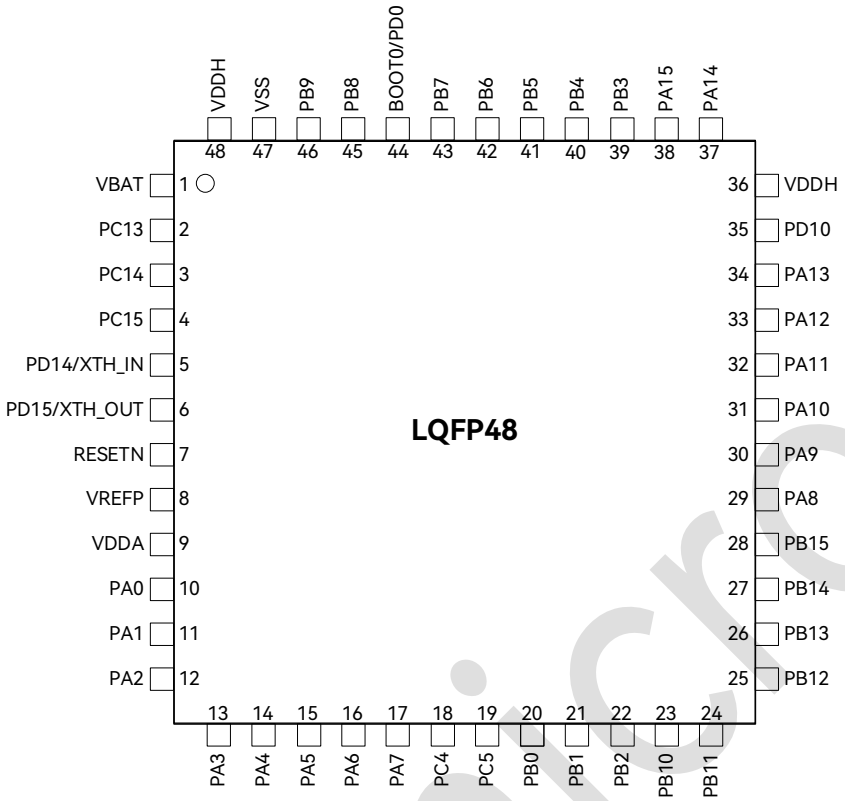

Figure 3-3: LQFP48 (7 * 7 mm) Pinout Diagram

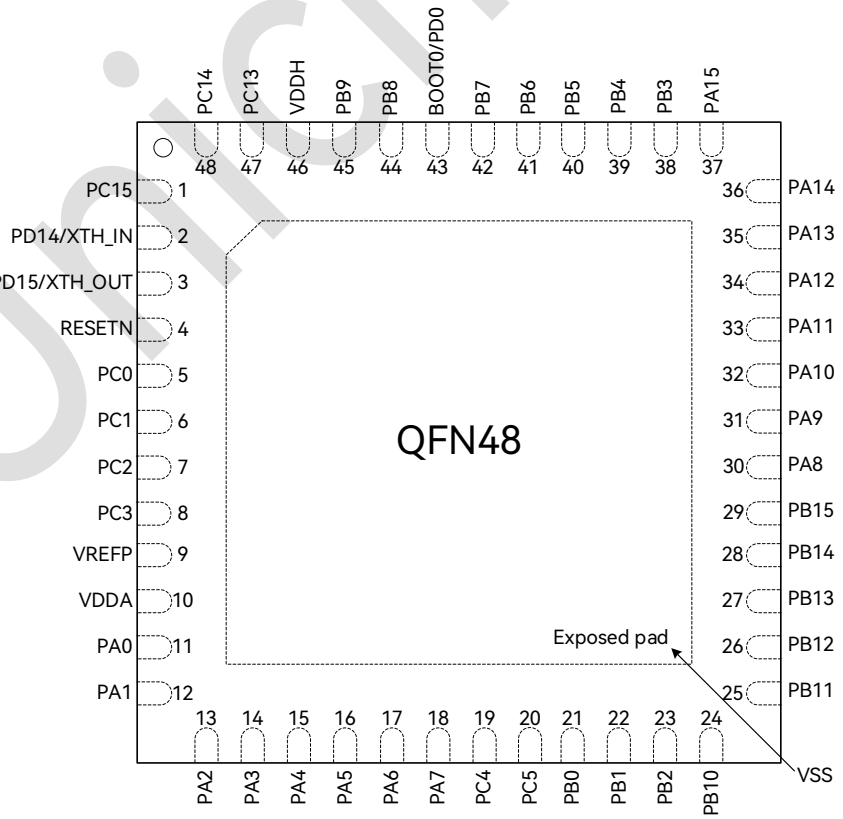

Figure 3-4: QFN48 (6 * 6 mm) Pinout Diagram

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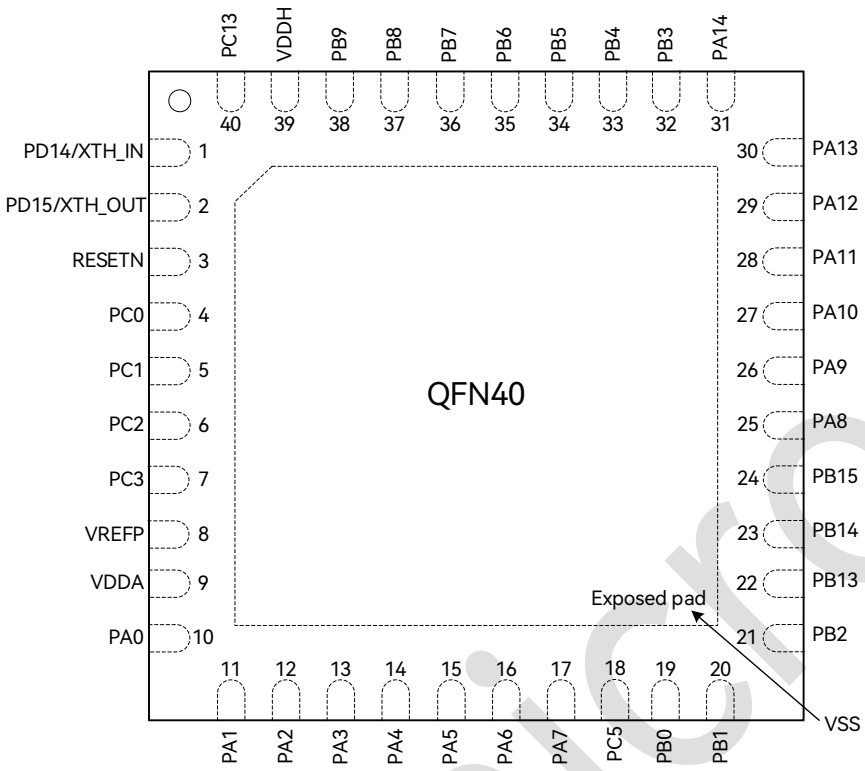

Figure 3-5: QFN40 (5 * 5 mm) Pinout Diagram

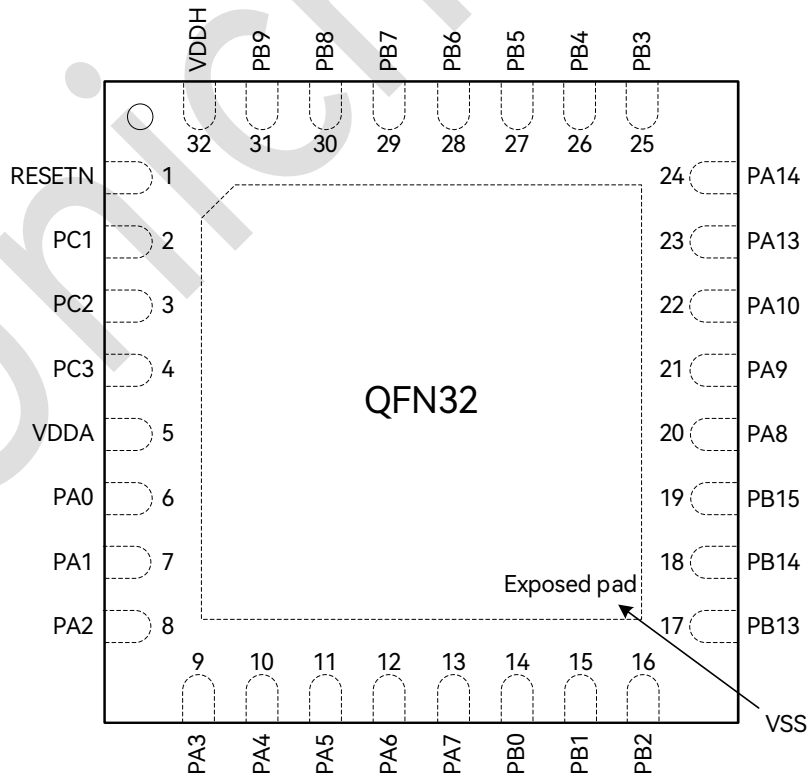

Figure 3-6: QFN32 (4 * 4 mm) Pinout Diagram

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3.2 Pin Description

Table 3-1: Abbreviation Definition

Name	Abbreviation	Definition
Pin Name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name.	
Type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O, fail-safe
	Tta	Fail-safe, 3.3 V tolerant I/O, directly connected to ADC, etc.
	B	Dedicated BOOT0 pin
	RST	Input reset pin with embedded weak pull-up resistor
Alternate function	Function selected through GPIOx_AFR registers	
Additional function	Function directly selected/enabled through peripheral registers	
Description	Unless otherwise specified by a note, all I/Os are set as floating inputs (high-impedance analog configuration) during and after reset.	

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Table 3-2: Pin Definition

Pin No.						Pin Name (Function after Reset)	Type	I/O Structure	Fail-safe	Pin Function		Description
LQFP64-0	LQFP64-1	LQFP48	QFN48	QFN40	QFN32					Alternate Function	Additional Function	
1	1	1	-	-	-	VBAT	S	-	-	-	-	When this pin is not in use, connect an external capacitor to ground or VDDH.
2	2	2	47	40	-	PC13-TAMPER-RTC	I/O	Tta	Yes	EVENTOUT	TAMPER-RTC/ WKUP	RESETN = 0, internal pull down
3	3	3	48	-	-	PC14-XTL_IN	I/O	Tta	Yes	-	XTL_IN	-
4	4	4	1	-	-	PC15-XTL_OUT	I/O	Tta	Yes	-	XTL_OUT	-
5	5	5	2	1	-	PD14-XTH_IN	I/O	Tta	-	TIM3_CH3/I2C1_SDA/ USART6_TX	XTH_IN	-
6	6	6	3	2	-	PD15-XTH_OUT	I/O	Tta	-	TIM3_CH4/I2C1_SCL/ USART6_RX	XTH_OUT	-
7	7	7	4	3	1	RESETN	I	RST	-	-	-	Pull-up by default
8	8	-	5	4	-	PC0	I/O	Tta	Yes	LPTIM0_IN/TIM4_CH1/ I2C0_SCL/UART1_TX/ USART6_TX/USART6_CTS/I2C2_SCL/ SPI0_SSN2/TIM9_ETR/EVENTOUT	ADC_IN10/ OPA1_VINP1/ TAMPER-RTC	-
9	9	-	6	5	2	PC1	I/O	Tta	Yes	LPTIM0_OUT/TIM4_CH2/I2C0_SDA/ SPI2_MOSI/UART1_RX/USART6_RX/ USART6_RTS/I2C2_SDA/SPI1_MOSI/ SPI0_MOSI/EVENTOUT	ADC_IN11/ OPA1_VINM1	-
10	10	-	7	6	3	PC2	I/O	Tta	Yes	TIM4_CH3/SPI1_MISO/I2S_EXTSD/ LPUART0_RX/USART6_TX	ADC_IN12/ OPA0_VINP1/ ACMP2_INP1	-

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Pin No.						Pin Name (Function after Reset)	Type	I/O Structure	Fail-safe	Pin Function		Description
LQFP64-0	LQFP64-1	LQFP48	QFN48	QFN40	QFN32					Alternate Function	Additional Function	
11	11	-	8	7	4	PC3	I/O	Tta	Yes	LPTIM0_TRIG/TIM4_CH4/SPI1_MOSI/ I2S_SD/USART6_RX	ADC_IN13/ OPA0_VINM1/ ACMP2_INM	-
12	12	8	9	8	-	VREFP (VREF+)	S	-	-	-	-	VREF+ is the same as VREFP. This pin can be connected to an external capacitor. It can use the internal 1.5/2/2.5/3V reference voltage of the chip or directly input an external reference voltage.
13	13	9	10	9	5	VDDA	S	-	-	-	-	If the VREFP pin is not used, this pin also serves as the reference voltage pin for VREF+.
14	14	10	11	10	6	PA0	I/O	Tta	Yes	ACMP0_OUT/TIM1_ETR/TIM4_CH1/ TIM7_ETR/I2C2_SCL/SPI0_MISO/ I2S_MCLK/UART1_CTS/UART3_TX/ USART6_CTSUSART6_RX/ LPUART0_RX/TIM0_ETR/TIM0_CH1/ TIM1_CH1/EVENTOUT	ADC_IN0/ OPA0_VINP0/ TAMPER-RTC	-
15	15	11	12	11	7	PA1	I/O	Tta	Yes	TIM1_CH2/TIM4_CH2/TIM14_CH1N/ I2C2_SDA/SPI0_SSN/SPI2_MOSI/ UART1_RTS/UART3_RX/USART6_RTS/ LPUART0_TX/TIM8_CH2/TIM0_CH1N/ TIM15_CH1/EVENTOUT	ADC_IN1/ OPA0_VINM0	-
16	16	12	13	12	8	PA2	I/O	Tta	Yes	ACMP1_OUT/TIM1_CH3/TIM4_CH3/ TIM14_CH1/I2C1_SDA/SPI0_MISO2/ UART1_TX/UART1_CTS/USART6_TX/ LPUART1_RX/TIM8_CH1/CAN0_RX/ TIM7_CH1/TIM7_BKIN	ADC_IN2/ OPA0_VOUT/ ACMP2_INP0/ TAMPER-RTC	-

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Pin No.						Pin Name (Function after Reset)	Type	I/O Structure	Fail-safe	Pin Function		Description
LQFP64-0	LQFP64-1	LQFP48	QFN48	QFN40	QFN32					Alternate Function	Additional Function	
17	17	13	14	13	9	PA3	I/O	Tta	Yes	TIM1_CH4/TIM4_CH4/TIM14_CH1N/ I2C1_SCL/SPI0_SSN2/UART1_RX/ UART1_RTS/USART6_RX/LPUART0_RX/ CAN0_TX/TIM7_CH2/TIM8_CH2	ADC_IN3/ OPA1_VOUT/ ACMP0_INP1	-
18/ 31/ 47/ 63	31 / 63	47	-	-	-	VSS	S	-	-	-	-	-
19/ 32/ 48/ 64	32 / 48 / 64	36/ 48	46	39	32	VDDH	S	-	-	-	-	-
-	18	-	-	-	-	PD9	I/O	Tta	Yes	TIM1_CH2/I2C2_SCL/SPI2_SCK/ SPI2_MOSI/UART2_RX/SPI2_SSN/ LPUART1_RX/SPI2_MISO	OPA1_VINP3/ ACMP2_INP3	
-	19	-	-	-	-	PD8	I/O	Tta	Yes	TIM1_CH1/I2C2_SDA/SPI2_SCK/ SPI2_MISO/UART2_TX/SPI2_SSN/ LPUART1_TX/SPI2_MOSI	OPA1_VINM3/ ACMP2_INP2	
20	20	14	15	14	10	PA4	I/O	Tta	Yes	LPTIM0_OUT/TIM0_CH3/TIM4_CH1/ I2C0_SCL/SPI0_SSN/SPI2_SSN/ UART0_TX/LPUART0_TX/USART6_CK/ SPI1_SSN/CAN0_RX/TIM7_CH3/ TIM3_CH3	ADC_IN4/ DAC_OUT/ ACMP0_INM/ ACMP1_INP0	-
21	21	15	16	15	11	PA5	I/O	Tta	Yes	LDO02_VOUT_OK/TIM1_ETR/TIM0_CH4 /TIM7_CH1N/I2C0_SDA/SPI0_SCK/ I2S_CK/UART0_RX/USART7_RX/ USART7_CK/LPTIM0_IN/CAN0_RX/	ADC_IN5/ OPA1_VINP0	-

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Pin No.						Pin Name (Function after Reset)	Type	I/O Structure	Fail-safe	Pin Function		Description
LQFP64-0	LQFP64-1	LQFP48	QFN48	QFN40	QFN32					Alternate Function	Additional Function	
										TIM1_CH1/TIM7_CH4/TIM3_CH4		
22	22	16	17	16	12	PA6	I/O	Tta	Yes	ACMP2_OUT/TIM0_BKIN/TIM2_CH1/ TIM7_BKIN/SPI0_MISO/I2S_MCLK/ UART1_TX/USART7_RX/USART7_CTS/ TIM8_CH3/TIM3_CH1/TIM15_CH1/ TIM7_CH3/TIM0_CH2N	ADC_IN6/ OPA1_VINM0	-
23	23	17	18	17	13	PA7	I/O	Tta	Yes	ACMP1_OUT/TIM0_CH1N/TIM2_CH2/ TIM7_CH1N/I2C1_SCL/SPI0_MOSI/ I2S_SD/UART1_RX/USART7_TX/ TIM4_CH1/TIM16_CH1/TIM3_CH1/ TIM0_CH4/EVENTOUT	ADC_IN7/ OPA2_VOUT/ ACMP1_INP1	-
24	24	18	19	-	-	PC4	I/O	FT	Yes	CLK1Hz/TIM3_CH1/TIM15_CH1/ I2C0_SCL/SPI1_MISO2/I2S_MCLK/ USART7_TX/USART6_CK/LPUART0_TX/ TIM9_CH1/LPUART1_TX/ TIM14_BKIN/EVENTOUT	ADC_IN14	-
25	25	19	20	18	-	PC5	I/O	FT	Yes	RTC_VLD_ON/TIM15_CH1N/I2C0_SDA/ SPI1_SSN2/USART7_RX/USART7_CTS/ LPUART0_RX/TIM9_CH2/LPUART1_RX	ADC_IN15	-
26	26	20	21	19	14	PB0	I/O	Tta	-	TIM0_CH2N/TIM2_CH3/TIM7_CH2N/ SPI0_MISO/UART3_TX/USART7_CK/ USART6_RX/LPUART1_TX/TIM9_CH1/ LPUART1_RX/TIM14_CH1/EVENTOUT	ADC_IN8/ OPA2_VINP0	-
27	27	21	22	20	15	PB1	I/O	Tta	Yes	TIM0_CH3N/TIM2_CH4/TIM7_CH3N/ TIM9_CH1/SPI0_MOSI/UART3_RX/ USART7_RTS/USART6_CK/SPI1_MOSI/ SPI1_SCK/SPI0_SCK/TIM4_CH1/ TIM3_CH2/EVENTOUT	ADC_IN9/ OPA2_VINM0/ ACMP1_INP2	-

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Pin No.						Pin Name (Function after Reset)	Type	I/O Structure	Fail-safe	Pin Function		Description
LQFP64-0	LQFP64-1	LQFP48	QFN48	QFN40	QFN32					Alternate Function	Additional Function	
28	28	22	23	21	16	PB2	I/O	Tta	Yes	LPTIM0_OUT/TIM2_ETR/TIM15_BKIN/ SPI0_MISO2/SPI2_MOSI/LPUART1_TX/ TIM9_CH3	ACMP1_INM ACMP0_INP0	BOOT1 as an input connected to pull-down resistor by default
29	29	23	24	-	-	PB10	I/O	Tta	Yes	ACMP2_OUT/TIM1_CH3/TIM3_ETR/ TIM0_CH4/I2C1_SCL/SPI1_SCK/I2S_CK/ UART2_TX/USART7_TX/USART7_RX/ UART1_TX/LPUART0_TX/I2C2_SCL/ LPUART0_RX/TIM8_CH3	ACMP0_INP2/ OPA2_VINP1	-
30	30	24	25	-	-	PB11	I/O	Tta	Yes	OPA0_OUT/TIM1_CH4/TIM4_ETR/ TIM0_CH3/I2C1_SDA/UART2_RX/ USART7_RX/USART7_TX/UART1_RX/ LPUART0_RX/I2C2_SDA/LPUART0_TX/ EVENTOUT	OPA2_VINM1	-
33	33	25	26	-	-	PB12	I/O	FT	Yes	OPA1_OUT/TIM0_BKIN/TIM4_CH1/ TIM0_CH1/I2C1_SDA/SPI1_SSN/I2S_WS /USART7_CK/CAN0_RX/SPI2_SSN/ LPUART1_TX/TIM8_CH4/TIM14_BKIN/ EVENTOUT	-	-
34	34	26	27	22	17	PB13	I/O	FT	Yes	OPA2_OUT/TIM0_CH1N/TIM4_CH2/ TIM9_CH3/I2C1_SCL/SPI1_SCK/I2S_CK/ UART1_CTS/USART7_CTS/CAN0_TX/ I2C1_SDA/LPUART1_RX/SPI2_SCK/ TIM8_CH4/TIM14_CH1N	-	-
35	35	27	28	23	18	PB14	I/O	FT	Yes	TIM0_CH2N/TIM0_CH1/TIM7_CH2N/ I2C1_SCL/SPI1_MISO/I2S_EXTSD/ UART1_RTS/USART7_RTS/I2C1_SDA/ UART3_TX/SPI2_MISO/TIM7_CH1/ TIM14_CH1	-	-

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Pin No.						Pin Name (Function after Reset)	Type	I/O Structure	Fail-safe	Pin Function		Description
LQFP64-0	LQFP64-1	LQFP48	QFN48	QFN40	QFN32					Alternate Function	Additional Function	
36	36	28	29	24	19	PB15	I/O	FT	Yes	TIM0_CH3N/TIM0_CH2N/TIM7_CH3N/ I2C1_SDA/SPI1_MOSI/I2S_SD/TIM8_ETR /SPI2_MOSI/UART3_RX/TIM7_CH1N/ TIM7_CH2/TIM15_CH1N	-	-
37	37	-	-	-	-	PC6	I/O	FT	Yes	TIM2_CH1/TIM7_CH1/I2C0_SCL/ I2S_MCLK/SPI1_SSN/USART7_TX/ CAN0_TX	-	-
38	38	-	-	-	-	PC7	I/O	FT	Yes	TIM2_CH2/TIM7_CH2/I2C0_SDA/ SPI1_SCK/USART7_RX/CAN0_RX/ EVENTOUT	-	-
39	39	-	-	-	-	PC8	I/O	FT	Yes	TIM2_CH3/TIM7_CH3/SPI1_MISO/ USART7_CK/CAN0_TX/LPTIM1_IN	-	-
40	40	-	-	-	-	PC9	I/O	FT	Yes	MCO1/TIM2_CH4/TIM7_CH4/I2C2_SDA/ SPI1_MOSI/USART7_RTS/CAN0_RX/ I2C1_SDA/LPTIM1_TRIG	-	-
41	41	29	30	25	20	PA8	I/O	FT	Yes	MCO0/TIM0_CH1/I2C2_SCL/SPI0_SSN/ I2S_WS/USART6_TX/LPUART1_RX/ I2C1_SDA/TIM0_CH2	-	-
42	42	30	31	26	21	PA9	I/O	FT	Yes	TIM0_CH2/TIM0_CH1/TIM14_BKIN/ I2C2_SDA/SPI1_MISO/UART0_TX/ UART1_TX/UART1_RX/I2C0_SCL/ SPI2_SCK/I2C1_SCL/TIM7_BKIN/ TIM0_CH3N	-	-
43	43	31	32	27	22	PA10	I/O	FT	Yes	TIM0_CH3/TIM7_CH1/TIM16_BKIN/ I2C1_SDA/SPI0_SCK/SPI1_SCK/ UART0_RX/UART1_RX/UART1_TX/ I2C0_SDA/SPI2_MOSI/TIM0_BKIN	-	-

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Pin No.						Pin Name (Function after Reset)	Type	I/O Structure	Fail-safe	Pin Function		Description
LQFP64-0	LQFP64-1	LQFP48	QFN48	QFN40	QFN32					Alternate Function	Additional Function	
44	44	32	33	28	-	PA11	I/O	Tta	-	ACMP0_OUT/TIM0_CH4/TIM3_ETR/ I2C1_SCL/SPI1_MISO/UART1_TX/ CAN0_RX/USB0_DM/SPI2_SSN	-	-
45	45	33	34	29	-	PA12	I/O	Tta	-	ACMP1_OUT/TIM0_ETR/I2C1_SDA/ SPI1_MOSI/UART1_RX/CAN0_TX/ USB0_DP/SPI2_MISO/EVENTOUT	-	-
46	46	34	35	30	23	PA13	I/O	FT	Yes	JTMS/SWDIO/SPI1_MISO/SPI1_SSN/ UART1_RX/I2C2_SDA/SPI2_MISO	-	Default SWDIO with an internal pull-up resistor
-	47	35	-		-	PD10	-	FT	Yes	LPTIM1_IN/TIM1_CH3/I2C1_SCL/ SPI2_MOSI/SPI2_SSN/UART3_RX/ SPI2_MISO/I2C0_SCL/SPI2_SCK/ LPUART1_RX	-	-
49	49	37	36	31	24	PA14	I/O	FT	Yes	JTCK/SWCLK/I2C0_SDA/SPI1_MOSI/ UART1_TX/USART6_CK/USART6_TX/ I2C2_SCL/SPI2_MOSI	-	Default SWCLK with an internal pull-down resistor
50	50	38	37	-	-	PA15	I/O	FT	Yes	JTDI/TIM1_ETR/TIM7_ETR/TIM15_CH1N /I2C0_SCL/SPI0_SSN/SPI2_SSN/ USART6_CTS/USART6_RX/SPI1_SSN/ TIM9_CH2/TIM7_CH1N/TIM1_CH1	-	Default JTDI, internal pull-up resistor
51	51	-	-	-	-	PC10	I/O	FT	Yes	TIM7_CH1N/TIM16_BKIN/SPI2_SCK/ UART2_TX/UART3_TX/USART7_TX/ CAN0_TX/LPUART0_TX/TIM15_BKIN/ LPUART1_TX/TIM9_CH4/EVENTOUT	-	-
52	52	-	-	-	-	PC11	I/O	FT	Yes	TIM7_CH2N/TIM16_CH1/I2S_EXTSD/ SPI2_MISO/UART2_RX/UART3_RX/ USART7_RX/CAN0_RX/LPUART0_RX/ TIM9_CH4/LPUART1_RX/TIM9_CH3	-	-

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Pin No.						Pin Name (Function after Reset)	Type	I/O Structure	Fail-safe	Pin Function		Description
LQFP64-0	LQFP64-1	LQFP48	QFN48	QFN40	QFN32					Alternate Function	Additional Function	
53	53	-	-	-	-	PC12	I/O	FT	Yes	TIM9_ETR/TIM16_CH1N/I2C2_SCL/ SPI2_MOSI/USART7_CK/CAN0_TX/ LPUART0_TX/TIM7_CH3N/LPUART1_TX /TIM8_CH1/EVENTOUT	-	-
54	54	-	-	-	-	PD2	I/O	FT	Yes	LPTIM1_OUT/TIM2_ETR/TIM16_BKIN/ I2C2_SDA/UART1_RX/CAN0_RX/ TIM14_CH1/TIM0_ETR	-	-
55	55	39	38	32	25	PB3	I/O	FT	Yes	JTDO/TIM1_CH2/SPI0_SCK/SPI2_SCK/ UART1_CTS/USART7_CK/USART6_RTS/ I2S_CK/SPI1_SCK/TIM7_CH3N/ TIM15_CH1/EVENTOUT	-	Default JTDO, input floating
56	56	40	39	33	26	PB4	I/O	FT	Yes	NJTRST/TIM0_BKIN/TIM2_CH1/ TIM16_BKIN/I2C0_SDA/SPI0_MISO/ SPI2_MISO/UART2_TX/USART7_TX/ USART6_TX/SPI1_MISO/I2S_EXTSD/ TIM7_CH3	-	Default NJRST, input with an internal pull-up resistor
57	57	41	40	34	27	PB5	I/O	FT	Yes	LPTIM0_IN/TIM2_CH2/TIM15_BKIN/ I2C0_SDA/SPI0_MOSI/SPI2_MOSI/ UART1_RTS/USART7_RX/USART6_RX/ UART2_RX/SPI1_MOSI/I2S_SD/ TIM7_BKIN/TIM7_CH4	-	-
58	58	42	41	35	28	PB6	I/O	FT	Yes	ACMP0_OUT/TIM0_CH2N/TIM3_CH1/ LPTIM0_TRIG/I2C0_SCL/SPI0_SSN/ SPI2_SSN/UART0_TX/USART7_CTS/ CAN0_RX/SPI1_SCK/LPUART0_TX/ TIM16_CH1/TIM15_CH1N/TIM7_CH3N	-	-
59	59	43	42	36	29	PB7	I/O	FT	Yes	LPTIM1_OUT/TIM3_CH2/TIM16_CH1N/ I2C0_SDA/SPI1_MISOSPI2_SCK/	-	-

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Pin No.						Pin Name (Function after Reset)	Type	I/O Structure	Fail-safe	Pin Function		Description
LQFP64-0	LQFP64-1	LQFP48	QFN48	QFN40	QFN32					Alternate Function	Additional Function	
										UART0_RX/USART7_RTS/CAN0_TX/ LPUART0_RX/TIM16_CH1N/TIM7_ETR/ EVENTOUT		
60	60	44	43	-	-	BOOT0	I	B	Yes	-	-	Internal pull-down resistor
61	61	45	44	37	30	PB8	I/O	FT	Yes	ACMP0_OUT/TIM3_CH3/TIM15_CH1/ I2C0_SCL/SPI2_MISO/UART0_TX/ CAN0_RX/LPUART1_RX/UART2_TX/ TIM9_CH1/TIM7_CH3/TIM8_ETR	-	-
62	62	46	45	38	31	PB9	I/O	FT	Yes	ACMP1_OUT/TIM0_CH4/TIM3_CH4/ TIM16_CH1/UART2_RX/I2C0_SDA/ SPI1_SSN/I2S_WS/CAN0_TX/SPI2_MOSI /TIM8_CH2	-	-

Note: PC13, PC14 and PC15 are powered by the power switch. Due to the limited filling current capacity of this switch (3 mA), the following limitations exist when using PC13 to PC15 in output mode:

- The speed cannot exceed 2 MHz and the maximum load is 30 pF.
- Cannot be used as a current source (e.g. to drive led).

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3.3 Alternate Function

Table 3-3: Alternate Function of Port A

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
Port A	PA0	ACMP0_OUT	TIM1_ETR	TIM4_CH1	TIM7_ETR	I2C2_SCL	SPI0_MISO	I2S_MCLK	UART1_CTS	UART3_TX	USART6_CTS	USART6_RX	LPUART0_RX	TIM0_ETR	TIM0_CH1	TIM1_CH1	EVENTOUT
	PA1	-	TIM1_CH2	TIM4_CH2	TIM14_CH1N	I2C2_SDA	SPI0_SSN	SPI2_MOSI	UART1_RTS	UART3_RX	USART6_RTS	-	LPUART0_TX	TIM8_CH2	TIM0_CH1N	TIM15_CH1	EVENTOUT
	PA2	ACMP1_OUT	TIM1_CH3	TIM4_CH3	TIM14_CH1	I2C1_SDA	SPI0_MISO2	-	UART1_TX	UART1_CTS	USART6_TX	LPUART1_RX	TIM8_CH1	CAN0_RX	TIM7_CH1	TIM7_BKIN	-
	PA3	-	TIM1_CH4	TIM4_CH4	TIM14_CH1N	I2C1_SCL	SPI0_SSN2	-	UART1_RX	UART1_RTS	USART6_RX	-	LPUART0_RX	CAN0_TX	TIM7_CH2	TIM8_CH2	-
	PA4	-	LPTIM0_OUT	TIM0_CH3	TIM4_CH1	I2C0_SCL	SPI0_SSN	SPI2_SSN	UART0_TX	LPUART0_TX	USART6_CK	SPI1_SSN	CAN0_RX	-	TIM7_CH3	TIM3_CH3	-
	PA5	-	TIM1_ETR	TIM0_CH4	TIM7_CH1N	I2C0_SDA	SPI0_SCK	I2S_CK	UART0_RX	USART7_RX	USART7_CK	LPTIM0_IN	CAN0_RX	TIM1_CH1	TIM7_CH4	TIM3_CH4	-
	PA6	ACMP2_OUT	TIM0_BKIN	TIM2_CH1	TIM7_BKIN	-	SPI0_MISO	I2S_MCLK	UART1_TX	USART7_RX	USART7_CTS	TIM8_CH3	TIM3_CH1	TIM15_CH1	TIM7_CH3	TIM0_CH2N	-
	PA7	ACMP1_OUT	TIM0_CH1N	TIM2_CH2	TIM7_CH1N	I2C1_SCL	SPI0_MOSI	I2S_SD	UART1_RX	USART7_TX	-	-	TIM4_CH1	TIM16_CH1	TIM3_CH1	TIM0_CH4	EVENTOUT
	PA8	MCO0	TIM0_CH1	-	-	I2C2_SCL	SPI0_SSN	I2S_WS	-	-	USART6_TX	-	LPUART1_RX	I2C1_SDA	-	TIM0_CH2	-
	PA9	-	TIM0_CH2	TIM0_CH1	TIM14_BKIN	I2C2_SDA	-	SPI1_MISO	UART0_TX	UART1_TX	UART1_RX	I2C0_SCL	SPI2_SCK	I2C1_SCL	TIM7_BKIN	TIM0_CH3N	-
	PA10	-	TIM0_CH3	TIM7_CH1	TIM16_BKIN	I2C1_SDA	SPI0_SCK	SPI1_SCK	UART0_RX	UART1_RX	UART1_TX	I2C0_SDA	SPI2_MOSI	-	-	TIM0_BKIN	-
	PA11	ACMP0_OUT	TIM0_CH4	TIM3_ETR	-	I2C1_SCL	-	SPI1_MISO		UART1_TX	CAN0_RX	USB0_DM	SPI2_SSN	-	-	-	-
	PA12	ACMP1_OUT	TIM0_ETR	-	-	I2C1_SDA	-	SPI1_MOSI	-	UART1_RX	CAN0_TX	USB0_DP	SPI2_MISO	-	-	-	EVENTOUT
	PA13	JTMS SWDIO	-	-	-	-	SPI1_MISO	SPI1_SSN	UART1_RX	-	-	I2C2_SDA	SPI2_MISO	-	-	-	-
	PA14	JTCK SWCLK	-	-	-	I2C0_SDA	-	SPI1_MOSI	UART1_TX	USART6_CK	USART6_TX	I2C2_SCL	SPI2_MOSI	-	-	-	-
	PA15	JTDI	TIM1_ETR	TIM7_ETR	TIM15_CH1N	I2C0_SCL	SPI0_SSN	SPI2_SSN	-	USART6_CTS	USART6_RX	-	SPI1_SSN	TIM9_CH2	TIM7_CH1N	TIM1_CH1	-

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Table 3-4: Alternate Function of Port B

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
Port B	PB0	-	TIM0_CH2N	TIM2_CH3	TIM7_CH2N	-	SPI0_MISO	-	UART3_TX	USART7_CK	USART6_RX	-	LPUART1_TX	TIM9_CH1	LPUART1_RX	TIM14_CH1	EVENTOUT
	PB1	-	TIM0_CH3N	TIM2_CH4	TIM7_CH3N	TIM9_CH1	SPI0_MOSI	-	UART3_RX	USART7_RTS	USART6_CK	SPI1_MOSI	SPI1_SCK	SPI0_SCK	TIM4_CH1	TIM3_CH2	EVENTOUT
	PB2	-	LPTIM0_OUT	TIM2_ETR	TIM15_BKIN	-	SPI0_MISO2	SPI2_MOSI	-	-	-	-	LPUART1_TX	-	-	TIM9_CH3	-
	PB3	JTDO	TIM1_CH2	-	-	-	SPI0_SCK	SPI2_SCK	UART1_CTS	USART7_CK	USART6_RTS	I2S_CK	SPI1_SCK	-	TIM7_CH3N	TIM15_CH1	EVENTOUT
	PB4	NJTRST	TIM0_BKIN	TIM2_CH1	TIM16_BKIN	I2C0_SDA	SPI0_MISO	SPI2_MISO	UART2_TX	USART7_TX	USART6_TX	-	SPI1_MISO	I2S_EXTSD	TIM7_CH3	-	-
	PB5	-	LPTIM0_IN	TIM2_CH2	TIM15_BKIN	I2C0_SDA	SPI0_MOSI	SPI2_MOSI	UART1_RTS	USART7_RX	USART6_RX	UART2_RX	SPI1_MOSI	I2S_SD	TIM7_BKIN	TIM7_CH4	-
	PB6	ACMP0_OUT	TIM0_CH2N	TIM3_CH1	LPTIM0_TRIG	I2C0_SCL	SPI0_SSN	SPI2_SSN	UART0_TX	USART7_CTS	CAN0_RX	SPI1_SCK	LPUART0_TX	TIM16_CH1	TIM15_CH1N	TIM7_CH3N	-
	PB7	-	LPTIM1_OUT	TIM3_CH2	TIM16_CH1N	I2C0_SDA	SPI1_MISO	SPI2_SCK	UART0_RX	USART7_RTS	CAN0_TX	-	LPUART0_RX	TIM16_CH1N	TIM7_ETR	-	EVENTOUT
	PB8	ACMP0_OUT	-	TIM3_CH3	TIM15_CH1	I2C0_SCL	-	SPI2_MISO	UART0_TX	-	CAN0_RX	UART2_TX	LPUART1_RX	TIM9_CH1	TIM7_CH3	TIM8_ETR	-
	PB9	ACMP1_OUT	TIM0_CH4	TIM3_CH4	TIM16_CH1	I2C0_SDA	SPI1_SSN	I2S_WS	-	-	CAN0_TX	UART2_RX	SPI2_MOSI	-	-	TIM8_CH2	-
	PB10	ACMP2_OUT	TIM1_CH3	TIM3_ETR	TIM0_CH4	I2C1_SCL	SPI1_SCK	I2S_CK	UART2_TX	USART7_TX	USART7_RX	UART1_TX	LPUART0_TX	I2C2_SCL	LPUART0_RX	TIM8_CH3	-
	PB11	OPA0_OUT	TIM1_CH4	TIM4_ETR	TIM0_CH3	I2C1_SDA	-	-	UART2_RX	USART7_RX	USART7_TX	UART1_RX	LPUART0_RX	I2C2_SDA	LPUART0_TX	-	EVENTOUT
	PB12	OPA1_OUT	TIM0_BKIN	TIM4_CH1	TIM0_CH1	I2C1_SDA	SPI1_SSN	I2S_WS	-	USART7_CK	CAN0_RX	SPI2_SSN	LPUART1_TX	TIM8_CH4	-	TIM14_BKIN	EVENTOUT
	PB13	OPA2_OUT	TIM0_CH1N	TIM4_CH2	TIM9_CH3	I2C1_SCL	SPI1_SCK	I2S_CK	UART1_CTS	USART7_CTS	CAN0_TX	I2C1_SDA	LPUART1_RX	SPI2_SCK	TIM8_CH4	TIM14_CH1N	-
	PB14	-	TIM0_CH2N	TIM0_CH1	TIM7_CH2N	I2C1_SCL	SPI1_MISO	I2S_EXTSD	UART1_RTS	USART7_RTS	-	I2C1_SDA	UART3_TX	SPI2_MISO	TIM7_CH1	TIM14_CH1	-
	PB15	-	TIM0_CH3N	TIM0_CH2N	TIM7_CH3N	I2C1_SDA	SPI1_MOSI	I2S_SD	-	-	TIM8_ETR	SPI2_MOSI	UART3_RX	TIM7_CH1N	TIM7_CH2	TIM15_CH1N	-

Table 3-5: Alternate Function of Port C

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
Port C	PC0	-	LPTIM0_IN	TIM4_CH1	-	I2C0_SCL	-	-	UART1_TX	USART6_TX	USART6_CTS	I2C2_SCL	-	SPI0_SSN2	-	TIM9_ETR	EVENTOUT
	PC1	-	LPTIM0_OUT	TIM4_CH2	-	I2C0_SDA	-	SPI2_MOSI	UART1_RX	USART6_RX	USART6_RTS	I2C2_SDA	SPI1_MOSI	SPI0_MOSI	-	-	EVENTOUT
	PC2	-	-	TIM4_CH3	-	-	SPI1_MISO	I2S_EXTSD	-	LPUART0_RX	USART6_TX	-	-	-	-	-	-
	PC3	-	LPTIM0_TRIG	TIM4_CH4	-	-	SPI1_MOSI	I2S_SD	-	-	USART6_RX	--	-	-	-	-	-
	PC4	CLK1Hz	-	TIM3_CH1	TIM15_CH1	I2C0_SCL	SPI1_MISO2	I2S_MCLK	-	USART7_TX	USART6_CK	-	LPUART0_TX	TIM9_CH1	LPUART1_TX	TIM14_BKIN	EVENTOUT
	PC5	RTC_VLD_ON	-	-	TIM15_CH1N	I2C0_SDA	SPI1_SSN2	-	-	USART7_RX	USART7_CTS	-	LPUART0_RX	TIM9_CH2	LPUART1_RX	-	-
	PC6	-	-	TIM2_CH1	TIM7_CH1	I2C0_SCL	I2S_MCLK	SPI1_SSN	-	-	USART7_TX	-	CAN0_TX	-	-	-	-
	PC7	-	-	TIM2_CH2	TIM7_CH2	I2C0_SDA	-	SPI1_SCK	-	-	USART7_RX	-	CAN0_RX	-	-	-	EVENTOUT
	PC8	-	-	TIM2_CH3	TIM7_CH3	-	-	SPI1_MISO	-	-	USART7_CK	-	CAN0_TX	-	LPTIM1_IN	-	-
	PC9	MCO1	-	TIM2_CH4	TIM7_CH4	I2C2_SDA	-	SPI1_MOSI	-	-	USART7_RTS	-	CAN0_RX	I2C1_SDA	LPTIM1_TRIG	-	-
	PC10	-	-	TIM7_CH1N	TIM16_BKIN	-	-	SPI2_SCK	UART2_TX	UART3_TX	USART7_TX	CAN0_TX	LPUART0_TX	TIM15_BKIN	LPUART1_TX	TIM9_CH4	-
	PC11	-	-	TIM7_CH2N	TIM16_CH1	-	I2S_EXTSD	SPI2_MISO	UART2_RX	UART3_RX	USART7_RX	CAN0_RX	LPUART0_RX	TIM9_CH4	LPUART1_RX	TIM9_CH3	-
	PC12	-	-	TIM9_ETR	TIM16_CH1N	I2C2_SCL	-	SPI2_MOSI	-		USART7_CK	CAN0_TX	LPUART0_TX	TIM7_CH3N	LPUART1_TX	TIM8_CH1	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

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Table 3-6: Alternate Function of Port D

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
Port D	PD2	-	LPTIM1_OUT	TIM2_ETR	TIM16_BKIN	I2C2_SDA	-	-	-	UART1_RX	-	CAN0_RX	-	-	TIM14_CH1	TIM0_ETR	-
	PD8	-	TIM1_CH1	-	-	I2C2_SDA	SPI2_SCK	SPI2_MISO	UART2_TX	-	-	SPI2_SSN	LPUART1_TX	SPI2_MOSI	-	-	-
	PD9	-	TIM1_CH2	-	-	I2C2_SCL	SPI2_SCK	SPI2_MOSI	UART2_RX	-	-	SPI2_SSN	LPUART1_RX	SPI2_MISO	-	-	-
	PD10	-	LPTIM1_IN	TIM1_CH3	-	I2C1_SCL	SPI2_MOSI	SPI2_SSN	UART3_RX	-	-	SPI2_MISO	I2C0_SCL	SPI2_SCK	LPUART1_RX	-	-
	PD14	-	-	TIM3_CH3	-	I2C1_SDA	-	-	-	USART6_TX	-	-	-	-	-	-	-
	PD15	-	-	TIM3_CH4	-	I2C1_SCL	-	-	-	USART6_RX	-	-	-	-	-	-	-

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4 Electrical Characteristics

4.1 Test Condition

Unless otherwise specified, all voltages are referenced to V_{ss}.

4.1.1 Minimum and Maximum Values

Unless otherwise specified, all products are tested on the production line at T_A = 25℃. The maximum and minimum values support the worst-case environmental temperature, supply voltage, and clock frequency as specified.

Notes below each table indicate that data are obtained through comprehensive evaluation, design simulation, or process characteristics, and not tested on the production line. Based on comprehensive evaluation, the maximum and minimum values are derived from sample testing by taking the average value and adding or subtracting three times the standard deviation (average ± 3σ).

4.1.2 Typical Value

Unless otherwise specified, typical data are measured based on T_A = 25 ℃ and V_{DDH} = V_{DDA} = 3.3 V. They are given only as design guidelines.

4.1.3 Typical Curve

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

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4.1.4 Power Supply Scheme

The chip supports single power supply and VBAT backup power supply. It requires an external operating supply voltage between 1.8 V and 3.6 V, and a digital circuit operating voltage generated by the built-in LDO.

The system power supply scheme is shown below.

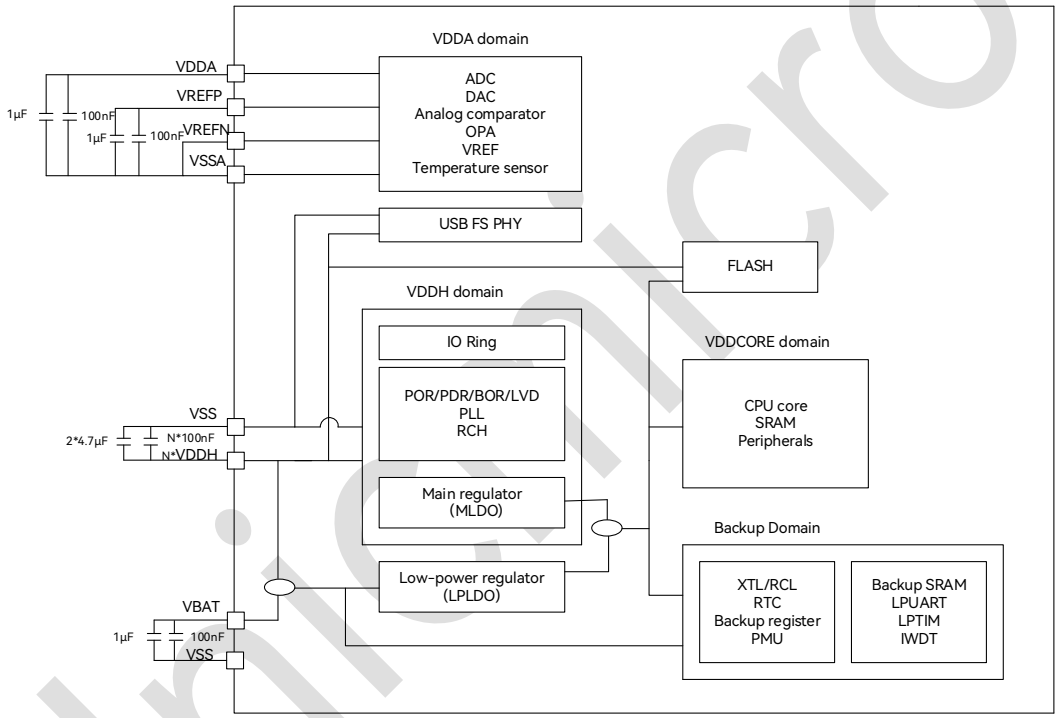

Figure 4-1: Block Diagram of Power Supply Scheme

Note: For multiple VDDH pins, it is recommended to add at least two 4.7 μF capacitors and N 100 nF capacitors in total. For each VDDH pin, at least one 100 nF capacitor is required. If the package has only one VDDH pin, two 4.7 μF capacitors and two 100 nF capacitors are required.

4.2 Absolute Maximum Ratings

Stresses above the absolute maximum ratings listed in Table 4-1, Table 4-2 and Table 4-3 may cause permanent damage to the device. These are stress ratings only and functional operation

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of the device at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1: Voltage Characteristics

Symbol	Description	Min.	Max.	Unit
$V_{DDH} - V_{SS}$	External main supply voltage (including V_{DDA} and V_{DDH}) (1)	-0.3	4	V
V_{IN}	Input voltage on 5 V tolerant pin (3)	$V_{SS} - 0.3$	5.5	
	Input voltage on other pins (2)	$V_{SS} - 0.3$	$V_{DDH} + 0.3$	
$\|\Delta V_{DDx}\|$	Variations between different V_{DDX} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all different ground pins	-	50	

Notes:

1. All main power (V_{DDH}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

2. V_{IN} shall not exceed its maximum value. Refer to Table 4-2 for current characteristics.

3. When a 5.5 V voltage is applied to the 5 V tolerant pin, V_{DDH} shall not be lower than 2.25 V.

Table 4-2: Current Characteristics

Symbol	Description	Max. (1)	Unit
I_{VDDH}	Total current into sum of all V_{DDH}/V_{DDA} power lines (source) (1) (3)	200	mA
I_{VSS}	Total current out of sum of all V_{SS} ground lines (sink) (1) (3)	200	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current sourced by any I/O and control pin	-20	
$I_{INJ(PIN)}$ (2)	Injected current on NRST pin	-5	
	Injected current on other pins	±5	

Notes:

1. All main power (V_{DDH}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.

2. A positive injection is induced by $V_{IN} > V_{DDH}$, and a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ maximum must always be respected. Refer to Table 4-1 for the maximum allowed

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injected current values.

3. When the maximum current occurs, the maximum voltage drop of V_{DDH} is allowed to be $0.1V_{DDH}$.

Table 4-3: Thermal Characteristics

Symbol	Description	Value	Unit
T_{stg}	Storage temperature range	-40–+150	℃

4.3 Operating Condition

Static parameter table (applicable temperature range: T_A = -40℃ – +105℃).

4.3.1 General Operating Condition

Table 4-4: General Operating Condition

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	168	204	MHz
f_{PCLK0}	Internal APB0 clock frequency	-	-	168	204	
f_{PCLK1}	Internal APB1 clock frequency	-	-	168	204	
V_{DDH}	Standard operating voltage	-	1.8	-	3.6	V
V_{DDA}	Analog operating voltage	Must be the same voltage as V_{DDH}	1.8	-	3.6	V
T_A	Ambient temperature	-	-40	-	105	℃

Notes:

1. It is recommended to power V_{DDH} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DDH} and V_{DDA} can be tolerated during power-up and normal operation.

2. Boost mode: The core operating voltage is 1.2 V, with a maximum operating frequency of 204 MHz.

3. Normal operating mode (default): The core operating voltage is 1.1 V, with a maximum operating frequency of 168 MHz.

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4.3.2 Operating Condition at Power-up / Power-down

Table 4-5: Operating Condition at Power-up / Power-down

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{VDDH}	V_{DDH} rise time rate	The supply voltage rises from 0 to V_{DDH}.	20	20000	μs/V
	V_{DDH} fall time rate	The supply voltage falls from V_{DDH} to 0.	80	20000	

4.3.3 Embedded Reset and Power Control Block Characteristics

Table 4-6: Embedded Reset and Power Control Block Characteristics

Symbol	Type	Condition	Typical	Unit
V_{PDR}	PDR rising trigger point	PDRS[1:0] = 00	1.57	V
		PDRS[1:0] = 01	1.77	
		PDRS[1:0] = 10	1.87	
		PDRS[1:0] = 11	1.97	
	PDR falling trigger point	PDRS[1:0] = 00	1.49	
		PDRS[1:0] = 01	1.67	
		PDRS[1:0] = 10	1.77	
		PDRS[1:0] = 11	1.87	
	Hysteresis voltage of PDR trigger point	PDRS[1:0] = 00	0.08	
		PDRS[1:0] = 01	0.1	
		PDRS[1:0] = 10	0.1	
		PDRS[1:0] = 11	0.1	
V_{BOR}	BOR trigger point	BORS[3:0] = 0000	1.56	V
		BORS[3:0] = 0001	1.66	
		BORS[3:0] = 0010	1.75	
		BORS[3:0] = 0011	1.85	
		BORS[3:0] = 0100	1.95	
		BORS[3:0] = 0101	2.05	
		BORS[3:0] = 0110	2.14	
		BORS[3:0] = 0111	2.24	
		BORS[3:0] = 1000	2.34	
		BORS[3:0] = 1001	2.43	
		BORS[3:0] = 1010	2.53	
		BORS[3:0] = 1011	2.63	
		BORS[3:0] = 1100	2.73	

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Symbol	Type	Condition	Typical	Unit
		BORS[3:0] = 1101	2.83	
		BORS[3:0] = 1110	2.92	
		BORS[3:0] = 1111	3.02	
V_{LVD}	LVD trigger point	LVDS[3:0] = 0000	1.59	V
		LVDS[3:0] = 0001	1.68	
		LVDS[3:0] = 0010	1.78	
		LVDS[3:0] = 0011	1.88	
		LVDS[3:0] = 0100	1.98	
		LVDS[3:0] = 0101	2.08	
		LVDS[3:0] = 0110	2.18	
		LVDS[3:0] = 0111	2.28	
		LVDS[3:0] = 1000	2.38	
		LVDS[3:0] = 1001	2.48	
		LVDS[3:0] = 1010	2.58	
		LVDS[3:0] = 1011	2.67	
		LVDS[3:0] = 1100	2.77	
		LVDS[3:0] = 1101	2.87	
		LVDS[3:0] = 1110	2.97	
		LVDS[3:0] = 1111	3.07	

Note: Guaranteed by design rather than test in production.

4.3.4 Embedded Voltage Reference

Table 4-7: Embedded Internal Voltage Reference

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REFINT}	Embedded Voltage Reference	VREF_SEL[1:0]=00, V_{DDA}>1.8V	TYP-0.9%	1.5	TYP+0.4%	V
		VREF_SEL[1:0]=01, V_{DDA}>2.5V	TYP-0.9%	2	TYP+0.4%	
		VREF_SEL[1:0]=10, V_{DDA} > 3V	TYP-0.9%	2.5	TYP+0.4%	
		VREF_SEL[1:0]=11, V_{DDA}>3.3V	TYP-0.9%	3	TYP+0.4%	
V_{cap}	External pin capacitance	-	-	1	-	μF

Notes:

1. To use the reference voltage output by internal V_{REF}, an external capacitor (typically 1 μF) must be connected to the V_{REFP} pin.

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2. The reference voltage output by internal V_{REF} is used as V_{REF} for the internal ADC/DAC/ACMP, etc.

3. If a precise V_{REF} input is provided externally (via pin V_{REFP}), the internal V_{REF} shall be turned off.

4.3.5 Supply Current Characteristics

Table 4-8: Supply Current Characteristics

Symbol	Parameter	Condition	f_{HCLK} (MHz)	Typical Value (V_{DDH} = 3.3 V)					Unit
				T_A = -40 ℃	T_A = 25 ℃	T_A = 85 ℃	T_A = 105 ℃	T_A = 125 ℃	
I_{DD-Run}	Supply current in run mode	All peripherals are enabled, the code runs: while (1) + memcopy in flash.	168	30.22	30.571	31.74	32.587	33.941	mA
			144	25.99	26.320	27.49	28.331	29.776	
			120	21.76	22.055	23.209	24.024	25.532	
			96	16.745	17.001	18.134	19.04	20.461	
			48	8.923	9.111	10.161	11.093	12.55	
			24	4.885	5.031	6.031	6.962	8.471	
			12	2.901	3.025	4.02	4.929	6.513	
		All peripherals are disabled, and only the EFC code runs: while (1) + memcopy in flash.	168	11.66	11.896	12.844	13.762	15.243	
			144	10.06	10.279	11.231	12.147	13.639	
			120	8.46	8.662	9.608	10.532	12.01	
			96	5.92	6.085	7.042	7.944	9.479	
			48	3.34	3.471	4.429	5.334	6.884	
			24	1.87	1.981	2.936	3.851	5.391	
			12	1.212	1.315	2.267	3.198	4.725	
	Supply current in run mode (boost mode)	All peripherals are enabled, the code runs: while (1) + memcopy in flash.	204	37.244	37.586	38.439	39.427	40.941	mA
			168	33.065	33.551	34.567	35.541	37.301	
			144	28.441	28.88	29.943	30.969	32.678	
			120	23.803	24.207	25.274	26.382	28.07	
			96	18.341	18.713	19.818	20.881	22.644	
			48	9.806	10.08	11.227	12.301	14.109	
			24	5.339	5.543	6.705	7.809	9.623	
			12	3.162	3.345	4.501	5.662	7.423	
		All peripherals are disabled, and only the EFC	204	18.711	19.012	20.08	21.17	22.73	
			168	11.864	12.206	13.361	14.438	16.330	
			144	10.241	10.553	11.704	12.797	14.632	

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Symbol	Parameter	Condition	f_{HCLK} (MHz)	Typical Value (V_{DDH} = 3.3 V)					Unit
				T_A = -40 ℃	T_A = 25 ℃	T_A = 85 ℃	T_A = 105 ℃	T_A = 125 ℃	
		code runs: while (1) + memcopy in flash.	120	8.612	8.904	10.054	11.144	12.978	
			96	5.872	6.131	7.268	8.383	10.171	
			48	3.378	3.586	4.721	5.844	7.634	
			24	1.966	2.152	3.301	4.416	6.227	
			12	1.278	1.451	2.610	3.711	5.561	
$I_{DD\text{-}Sleep}$	Supply current in Sleep mode	All peripherals are enabled, the code runs: while (1) + memcopy in flash.	168	22.24	22.58	23.87	25.15	27.03	mA
			144	19.13	19.45	20.75	22.01	23.88	
			120	16.018	16.32	17.63	18.91	20.78	
			96	12.15	12.42	13.72	15.04	16.89	
			48	6.51	6.74	8.06	9.038	11.28	
			24	3.65	3.87	5.21	6.53	8.46	
			12	2.24	2.45	3.78	5.08	7.04	
		All peripherals are disabled, and only the EFC code runs: while (1) + memcopy in flash.	168	5.01	5.258	6.62	7.86	9.88	mA
			144	4.35	4.59	5.95	7.21	9.23	
			120	3.69	3.92	5.26	6.52	8.57	
			96	2.11	2.30	3.65	4.90	6.94	
			48	1.3	1.48	2.84	4.09	6.12	
			24	0.9	1.08	2.42	3.68	5.71	
			12	0.69	0.87	2.21	3.48	5.5	

Notes:

1. APB0 = APB1 = AHB
2. f_{HCLK} > 96 MHz is derived from PLL0 multiplication and f_{HCLK} ≤ 96 MHz is derived from RCH division
3. PDR, BOR and LVD are disabled
4. Boost mode: core operating voltage 1.2 V
5. Normal operating mode: core operating voltage 1.1 V
6. Low voltage mode: core operating voltage 0.9 V

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Table 4-9: Typical Value in Low-power Mode

Symbol	Parameter	Condition	Typ.			Unit
			T_A = -40 ℃	T_A = 25 ℃	T_A = 105 ℃	
I_{DD_Stop}	Supply current in Stop mode	Low-speed clock is enabled, RTC is running, independent watchdog is enabled, and high-frequency clocks PLL/XTH/RCH are stopped. CPU, IO and SRAM are retained, and the program before wake-up (low-voltage operation) can be continued after a quick wake-up.	-	300	-	μA
	Supply current in Stop mode (0.9 V low-power mode)	Low-speed clock is enabled, RTC is running, independent watchdog is enabled, and high-frequency clocks PLL / XTH / RCH are stopped. CPU, IO and SRAM are retained, and the program before wake-up (low-voltage operation) can be continued after a quick wake-up.	-	170	-	μA
$I_{DD_Standby0}$	Supply current in Standby0 mode	External low-speed clock is enabled, RTC is running, backup registers and 8 KB backup SRAM are retained, independent watchdog is enabled,	-	5.5	-	μA

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Symbol	Parameter	Condition	Typ.			Unit
			T_A = -40 ℃	T_A = 25 ℃	T_A = 105 ℃	
		LPTIM0/LPTIM1 and LPUART are disabled.				
		External low-speed clock is enabled, RTC is running, backup registers and 8 KB backup SRAM are retained, independent watchdog is disabled, LPTIM0/LPTIM1 and LPUART are disabled.	-	5.3	-	μA
		Internal low-speed clock is enabled, RTC is running, backup registers and 8 KB backup SRAM are retained, independent watchdog is disabled, LPTIM0/LPTIM1 and LPUART are disabled.	-	5	-	μA
$I_{DD_Standby1}$	Supply current in Standby1 mode	External low-speed clock is enabled, RTC is running, backup registers are retained, 8 KB backup SRAM is not retained, independent watchdog is disabled, LPTIM0/LPTIM1 and LPUART are disabled.	-	2.3	-	μA
		Internal low-speed clock is enabled, RTC is running, backup registers are retained, 8 KB backup SRAM is not retained, independent	-	2	-	μA

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Symbol	Parameter	Condition	Typ.			Unit
			T_A = -40 ℃	T_A = 25 ℃	T_A = 105 ℃	
		watchdog is disabled, LPTIM0/LPTIM1 and LPUART are disabled.				
	Supply current in Standby1 mode (0.9 V low voltage mode)	Internal low-speed clock is enabled, RTC is running, backup registers are retained, 8 KB backup SRAM is not retained, independent watchdog is disabled, LPTIM0/LPTIM1 and LPUART are disabled.	-	1.5	-	μA
$I_{DD_DeepStandby0}$	Supply current in DeepStandby0 mode	Both external and internal low-speed clocks are disabled, RTC does not run, backup registers are retained, 8 KB backup SRAM is retained, and independent watchdog is disabled. Powered by V_{DDH}	-	4.5	-	μA
$I_{DD_DeepStandby1}$	Supply current in DeepStandby1 mode	Both external and internal low-speed clocks are disabled, RTC does not run, backup registers are retained, 8 KB backup SRAM is not retained, and independent watchdog is disabled. Powered by V_{DDH}	-	1.5	-	μA
$I_{DD_DeepStandby1}$ (VBAT)	Supply current in DeepStandby1 mode	Both external and internal low-speed clocks are disabled, RTC	-	1.11	-	μA

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Symbol	Parameter	Condition	Typ.			Unit
			T_A = -40 ℃	T_A = 25 ℃	T_A = 105 ℃	
		does not run, backup registers are retained, 8 KB backup SRAM is not retained, and independent watchdog is disabled. V_{DDH} is switched off; powered by V_{BAT}.				

4.3.6 External Clock Source Characteristics

4.3.6.1 High-speed External User Clock Generated from an External Source (HSE / XTH)

Table 4-10: HSE / XTH Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{XTH_IN}	Oscillator frequency	XTH_SF[1:0] = 00	1	-	4	MHz
		XTH_SF[1:0] = 01	4.1	-	12	
		XTH_SF[1:0] = 10	12.1	-	24	
		XTH_SF[1:0] = 11	24.1	-	48	

Notes:

1. The resonator characteristics are given by the crystal/ceramic resonator manufacturer.

2. Guaranteed by design rather than test in production.

4.3.6.2 External Low-speed Clock Source (LSE/XTL)

Table 4-11: LSE/XTL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{XTL_IN}	Oscillator frequency	-	-	32.768	-	kHz
$t_{SU(XTL)}$	Startup time	V_{DDH} is stabilized	-	500	-	ms

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Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{DD}	Operating current	-	-	200	-	nA
$C_{L1/CL2}$	External capacitance	-	-	20	-	pF

4.3.7 Internal Clock Source Characteristics

4.3.7.1 High-speed Internal RC Oscillator (RCH)

Table 4-12: RCH Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{RCH}	Frequency band	V_{DDH} = 3.3 V, T_A = 25℃, after calibration	-	96	-	MHz
ACC_{RCH}	Accuracy of RCH oscillator	V_{DDH} = 3.3 V, T_A = -40℃–105℃	-2.5	-	2.5	%
$t_{SU(RCH)}$	Startup time of RCH oscillator	-	-	16	-	μs
$I_{DD(RCH)}$	Current consumption of RCH oscillator	-	-	80	-	μA

4.3.7.2 Low-speed Internal RC Oscillator (RCL)

Table 4-13: RCL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{RCL}	Frequency band	V_{DDH} = 3.3 V, T_A = 25℃, after calibration	-	32	-	kHz
ACC_{RCL}	Accuracy of RCL oscillator	V_{DDH} = 3.3 V, T_A = -40℃–105℃	-2.5	-	2.5	%
$t_{SU(RCL)}$	Startup time of RCL oscillator	-	-	-	500	μs
$I_{DD(RCL)}$	Current consumption of RCL oscillator	-	-	200	-	nA

4.3.8 Wake-up Time from Low-power Mode

Table 4-14: Wake-up Time

Symbol	Parameter	Typical Value	Unit
$t_{WUSleep}$	Wake-up time from Sleep mode	5	HCLK

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Symbol	Parameter	Typical Value	Unit
t_{WUStop}	Wake-up time from Stop mode	3	μs
$t_{WUStandby0}$	Wake-up time from Standby0 mode	260	μs
$t_{WUStandby1}$	Wakeup time from Standby1 mode	350	μs

4.3.9 PLL Characteristics

Table 4-15: PLL Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{PLL_IN}	PLL reference input clock	0.9	-	100	MHz
	PLL input clock duty cycle	40	50	60	-
f_{VCO_OUT}	VCO output clock	300	-	700	MHz
f_{PLL_OUT}	PLL output clock ($f_{VCO_OUT/P}$)	42.9	-	700	MHz
t_{LOCK}	PLL lock time (reference input clock 4 MHz)	-	-	150	μs
Jitter	RMS (cycle-to-cycle jitter) @ PLL clock output 204 MHz (integer mode)	-	15	-	ps
Jitter	RMS (cycle-to-cycle jitter) @ PLL clock output 168 MHz (fractional mode or spread-spectrum mode)	-	18	-	ps
I_{PLL}	Operating current of PLL	-	-	0.5	mA

Notes:

1. Guaranteed by design rather than test in production.
2. Fractional frequency division can be used for audio and other applications.
3. Spread-spectrum function helps to reduce electromagnetic interference.

4.3.10 Flash Memory Characteristics

Table 4-16: Flash Memory Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{prog}	32-bit programming time	-	41	-	μs
t_{ERASE}	One page (4 Kbytes) erase time	-	12	16	ms
t_{ME}	Mass erase time	-	-	16	ms
N_{END}	Endurance (erase count)	-	-	10	kcycle
t_{RET}	Data retention	-	-	10	Year

Note: Guaranteed by characterization results rather than test in production.

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4.3.11 Absolute Maximum Ratings (Electrical Sensitivity)

Using specific measurement methods, the chip is stressed to determine its performance in terms of electrical sensitivity.

4.3.11.1 Electrostatic Discharge (ESD)

Table 4-17: ESD Characteristics

Symbol	Parameter	Condition	Class	Max.	Unit
$V_{ESD(HBM)}$	Electrostatic discharge (HBM)	T_A = 25℃, compliant with ESDA/JEDEC JS-001-2023	3 A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge (CDM)	T_A = 25℃, compliant with ESDA/JEDEC JS-002-2018	C3	1500	V

4.3.11.2 Static Latch-up (LU)

Table 4-18: LU Characteristics

Symbol	Parameter	Condition	Class	Max.	Unit
LU	Static latch-up class	T_A = +105℃, compliant with ESDA/JEDEC JESD78E-2016	Class II	200	mA

4.3.11.3 EFT

Table 4-19: EFT Characteristics

Symbol	Parameter	Condition	Type	Max.	Unit
EFT_{IO}	EFT to IO	IEC61000-4-4	4	2000	V
EFT_{Power}	EFT to Power	IEC61000-4-4	4	4000	V

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4.3.12 I/O Port Characteristics

Table 4-20: I/O DC Characteristics at 3.3 V V_{DDH}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage	-	V_{SS}	-	0.8	V
V_{IH}	Input high level voltage	-	2	-	V_{DDH}	
V_{OL}	Output low level voltage	-	V_{SS}	-	0.4	
V_{OH}	Output high level voltage	-	2.4	-	V_{DDH}	
V_{hys}	I/O Schmitt trigger voltage hysteresis	-	-	200	-	mV
I_{lkg}	Input leakage current	V_{DDH} = Maximum V_{PAD} = 0 or V_{PAD} = V_{DDH}	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistor	V_{DDH} = 3.3 V, V_{IN} = V_{SS}	9	-	19.4	kΩ
R_{PD}	Weak pull-down equivalent resistor	V_{DDH} = 3.3 V, V_{IN} = V_{DDH}	6.7	-	16	kΩ

Table 4-21: I/O DC Characteristics at 1.8 V V_{DDH}

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage	-	V_{SS}	-	0.3*V_{DDH}	V
V_{IH}	Input high level voltage	-	0.7*V_{DDH}	-	V_{DDH}	
V_{OL}	Output low level voltage	-	V_{SS}	-	0.2*V_{DDH}	
V_{OH}	Output high level voltage	-	0.8*V_{DDH}	-	V_{DDH}	
V_{hys}	I/O Schmitt trigger voltage hysteresis	-	-	0.1*V_{DDH}	-	mV
I_{lkg}	Input leakage current	V_{DDH} = Maximum V_{PAD} = 0 or V_{PAD} = V_{DDH}	-1	-	1	μA
R_{PU}	Weak pull-up equivalent resistor	V_{DDH} = 3.3 V, V_{IN} = V_{SS}	11.2	-	32.4	kΩ
R_{PD}	Weak pull-down equivalent resistor	V_{DDH} = 3.3 V, V_{IN} = V_{DDH}	9.4	-	32.4	kΩ

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4.3.13 ADC Electrical Characteristics

Table 4-22: ADC Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	Using external reference voltage	1.8	-	3.6	V
V_{REF+}	Positive reference voltage	-	1.8	-	V_{DDA}	V
V_{REF-}	Negative reference voltage	-	-	0	-	V
f_{ADC}	ADC clock frequency	-	-	-	84	MHz
f_s	Sampling rate	1.8 V ≤ V_{DDA} ≤ 3.6 V	-	-	5.25	Msps
Resolution	Resolution	-	-	12	-	bit
V_{AIN}	Conversion voltage range	-	0	-	V_{REF+}	V
R_{AIN}	External input impedance	Please refer to Table 4-23 for detailed information.	-	4206	-	Ohm
R_{ADC}	Sampling switch impedance	-	-	-	720	Ohm
C_{ADC}	Internal sampling and holding capacitance	-	-	5.58	-	pF
SNR	Signal-to-noise-and-distortion ratio	SNR @ 30 kHz	-	64	-	dB
THD	-	THD @ 30 kHz	-	-65	-	dB
DNL	-	DNL	-	-	2.5	LSB
INL	-	INL	-	-	5	LSB
ENOB	-	Single-ended ENOB @ 30 kHz	-	10.25	-	bit
		Differential ENOB @ 30 kHz	-	10.4	-	bit

Note: Guaranteed by design rather than test in production.

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Table 4-23: ADC External Input Impedance Parameter

ADC Clock	ADC Sampling Rate	Sampling Time（ns, fixed at 4 ADC clock cycles）	Maximum External Input Impedance (ohms, R_{AIN})
40 MHz	2.5 Msps	100	1129
30 MHz	1.875 Msps	133	1745
20 MHz	1.25 Msps	200	2975
15 MHz	0.9375 Msps	266	4206

4.3.14 DAC Electrical Characteristics

Table 4-234: DAC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	1.8	3.3	3.6	V
R_L	Load resistance when DAC output buffer is ON	5	-	-	kΩ
C_L	Load capacitance	-	-	50	pF
DAC_OUT	Voltage on DAC_OUT output when DAC output buffer is OFF	0	-	V_{REF+}	V
	Voltage on DAC_OUT output when DAC output buffer is ON	0.2	-	V_{REF+} - 0.2	V
V_{REF+}	-	TYP-0.1%	Optional 1.5 / 2.0 / 2.5 / 3.0 or V_{DDA}	TYP+0.1%	V
V_{REF-}	-	-	-	0	V
Resolution	Resolution	-	12	-	bit
f_s	Sampling rate	-	-	1	MHz
SNR	-	-	65	-	dB
THD	-	-	65	-	dB
DNL	Differential non linearity	-	2	-	LSB
INL	Integral non linearity	-	4	-	LSB

Note: Guaranteed by design rather than test in production.

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4.3.15 Operational Amplifier (OPA) Characteristics

Table 4-245: OPA Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DDA}	Operating voltage	1.8	-	3.6	V
T_A	Ambient temperature	-40	-	105	℃
I_{DDA}	Operating current	-	3	-	mA
C_{MIR}	Common mode input range	0	-	V_{DDA}	V
BW	Bandwidth	-	10	-	MHz
R_{LOAD}	Load resistance	600	-	-	Ω
C_{LOAD}	Load capacitance	-	6	30	pF
SR	Slew rate 2 V step 20% to 80% GAINSEL[2:0] = 000 Load capacitance: 5 pF	7.5	-	-	V/μs
e_n	Voltage noise density, @ 1 kHz, output loaded with 1 kΩ	-	91	-	nV/sqrt (Hz)
	Voltage noise density, @ 10 kHz, output loaded with 1 kΩ	-	33	-	nV/sqrt (Hz)
Mode	Supporting OPA operation Comparator mode Unit buffer mode Single-ended PGA mode	-	-	-	-

Note: Guaranteed by design rather than test in production.

4.3.16 Analog Comparator (ACMP) Electrical Characteristics

Table 4-256: ACMP Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{IN}	Input voltage range	-	0	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	-	10	μs
t_{DR}	Rising edge propagation delay	V_{DDA}=3.3 V, V_{IN}=5 mV	-	100	-	ns
t_{DF}	Falling edge propagation delay	V_{DDA}=3.3 V, V_{IN}=5 mV	-	100	-	ns

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Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OFFSET}	Comparator input offset error		-	-	±10	mV
V_{hys}	Comparator hysteresis voltage	CHYS[1:0] = 00	-	0	-	mV
		CHYS[1:0] = 01	-	10.5	-	mV
		CHYS[1:0] = 10	-	20.5	-	mV
		CHYS[1:0] = 11	-	30.5	-	mV
I_{DDA}	Operating current	Normal operation (CEN = 1, CLPM = 0)	-	-	5	μA

Note: Guaranteed by design rather than test in production.

4.3.17 Temperature Sensor (TS) Characteristics

Table 4-7: TS Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_L	VTS linearity with temperature	-	±1	±5	ºC
Avg_Slope	Average slope	-	-1.9	-	mV/ºC
t_{START}	Settling time	-	10	-	μs

Note: Guaranteed by characterization results rather than test in production.

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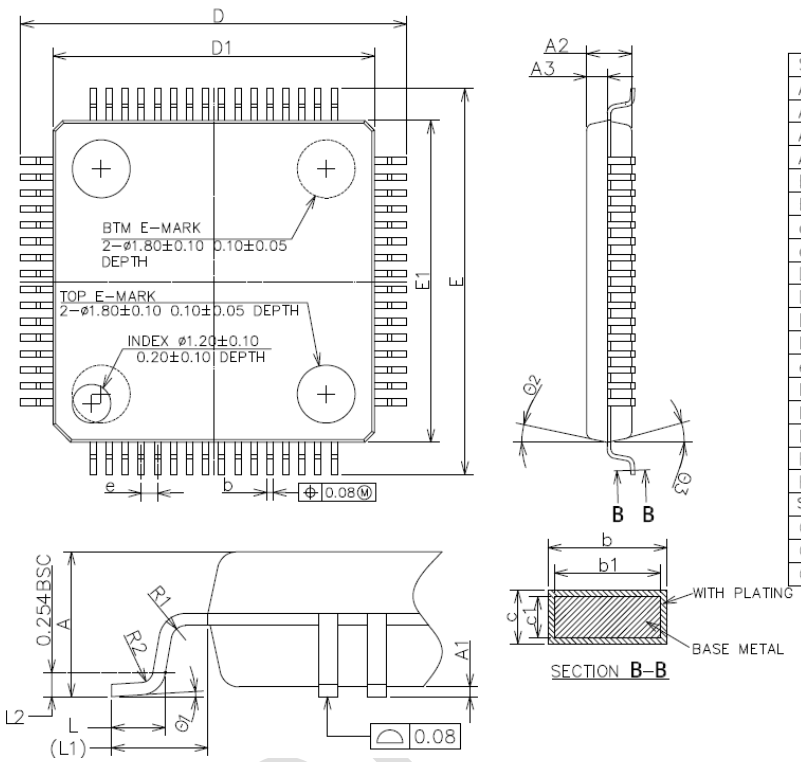
5 Package Outline

5.1 LQFP64 (10 * 10 mm)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.120	0.127	0.134
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.40	0.50	0.60
L	0.53	–	0.70
L1	1.0REF		
L2	0.254BSC		
R1	0.1REF		
R2	0.15REF		
S	0.262REF		
Θ1	0°	–	8°
Θ2	11°	12°	13°
Θ3	11°	12°	13°

Figure 5-1: LQFP64 (10 * 10 mm) Package Outline Drawing

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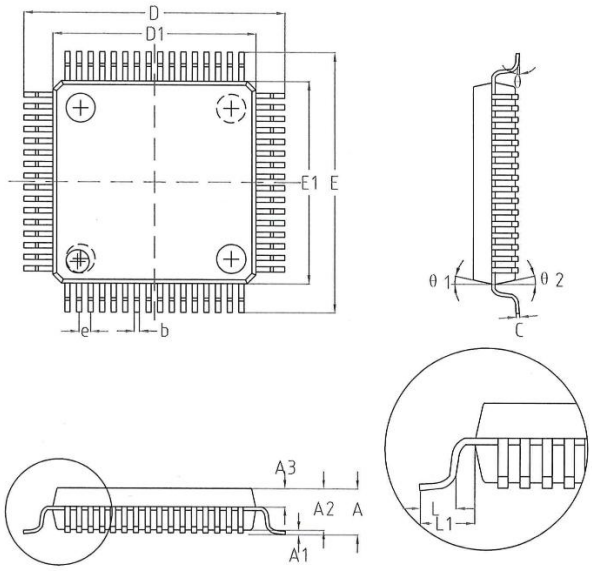
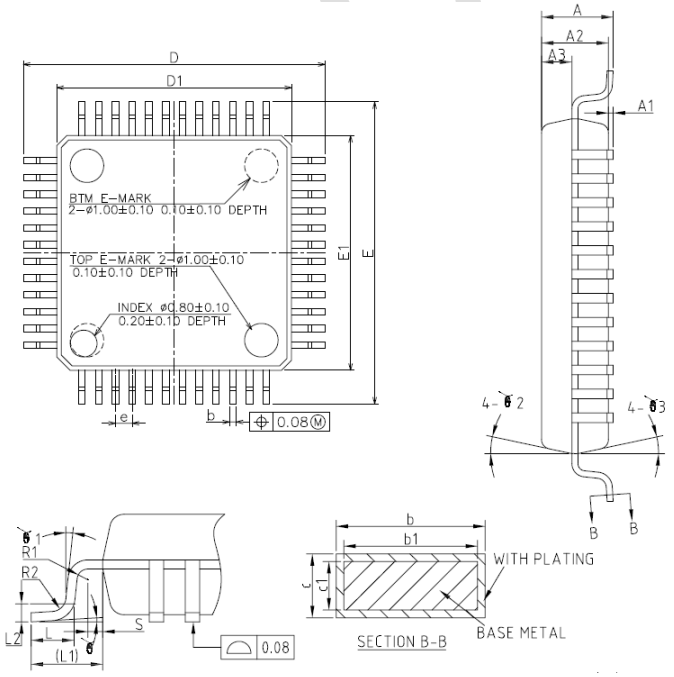
5.2 LQFP64 (7 * 7 mm)



机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.16	–	0.24
c	0.13	–	0.18
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0°	3.5°	7°
θ1	11°	12°	13°
θ2	11°	12°	13°

Figure 5-2: LQFP64 (7 * 7 mm) Package Outline

5.3 LQFP48 (7 * 7 mm)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.28
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40	0.50	0.60
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.254REF		
R1	0.12REF		
R2	0.15REF		
S	0.259REF		
θ1	0°	–	8°
θ2	11°	12°	13°
θ3	11°	12°	13°

Figure 5-3: LQFP48 (7 * 7 mm) Package Outline Drawing

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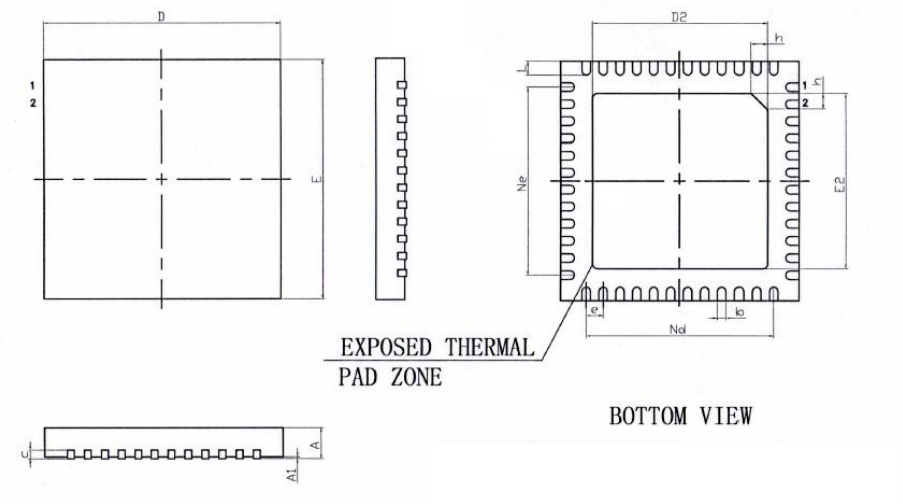
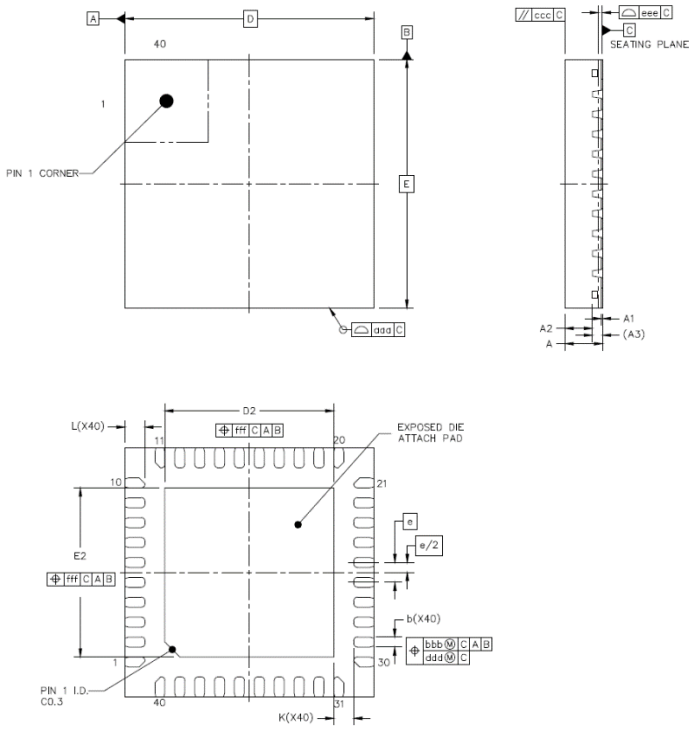
5.4 QFN48 (6 * 6 mm) (Reference)



SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.70	0.75	0.80	
A1	—	0.02	0.05	
b	0.15	0.20	0.25	1
c	0.18	0.20	0.23	
D	5.90	6.00	6.10	
D2	4.10	4.20	4.30	2
e	0.40BSC			
Ne	4.40BSC			
Nd	4.40BSC			
E	5.90	6.00	6.10	
E2	4.10	4.20	4.30	2
L	0.30	0.40	0.50	
h	0.30	0.35	0.40	
L/F载体尺寸 (MIL)	177*177			

Figure 5-4: QFN48 (6 * 6 mm) Package Outline Drawing

5.5 QFN40 (5 * 5 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	5 BSC		
	Y	E	5 BSC		
LEAD PITCH		e	0.4 BSC		
EP SIZE	X	D2	3.3	3.4	3.5
	Y	E2	3.3	3.4	3.5
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K	0.4 REF		
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		ccc	0.1		
COPLANARITY		eee	0.08		
LEAD OFFSET		bbb	0.07		
		ddd	0.05		
EXPOSED PAD OFFSET		fff	0.1		

Figure 5-5: QFN40 (5 * 5 mm) Package Outline Drawing

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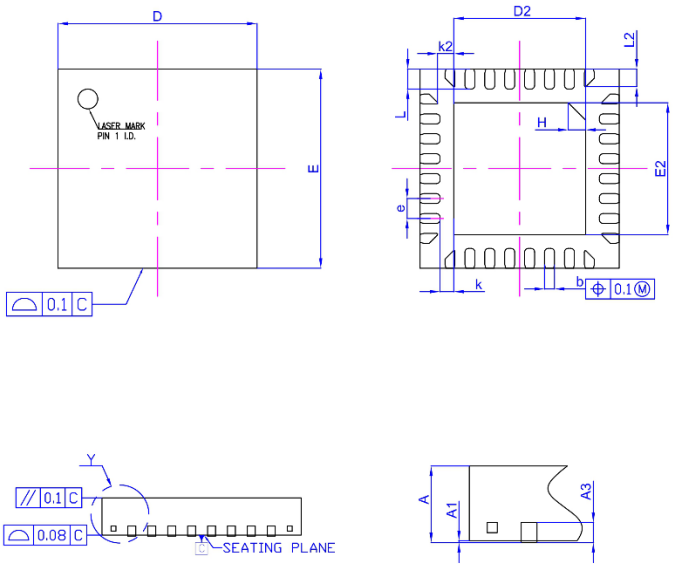
5.6 QFN32 (4 * 4 mm)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203REF	
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.55	2.65	2.75
E2	2.55	2.65	2.75
b	0.15	0.20	0.25
e		0.40BSC	
L	0.325	0.40	0.475
L2	0.275	0.35	0.425
k		0.275REF	
k2		0.325REF	
H		0.35REF	

Figure 5-6: QFN32 (4 * 4 mm) Package Outline Drawing

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6 Revision History

Version	Date	Modifications
V1.0	-	Initial release.
V1.0.1	-	1. Updated the descriptions of the table “Pin Definition”. 2. Updated the descriptions on the home page. 3. Updated the number of ACMPs in the “Configuration Table”. 4. Updated the descriptions of the chapter “Functional Overview”. 5. Updated some parameters of the table “Typical Value in Low-power Mode”.
V 1.1	-	1. Updated the table “Pin Description”. 2. Updated the LU level. 3. Updated the maximum value of clock frequency. 4. Updated the parameters of “Temperature Sensor (TS) Characteristics”. 5. Updated the Package outline drawings of QFN40, QFN48 and QFN32. 6. Deleted the junction temperature. 7. Updated the descriptions of the chapter “Functional Overview”.
V1.1.1	-	1. Updated the maximum clock frequency. 2. Updated the chapter “Supply Current Characteristics”.
V1.1.2	-	1. Added the section “Naming Convention”. 2. Updated the maximum accuracy values for RCH/RCL oscillators. 3. Added the power supply current parameters for Sleep mode.
V1.2	-	1. Modified the part no. suffix to “7”. 2. Updated the configuration table. 3. Updated the pin description table. 4. Updated the descriptions on the home page. 5. Deleted the PDR in reset mode table. 6. Updated HBM and CDM values and $V_{ESD(HBM)}$ level in the “Electrostatic Discharge (ESD)” section. 7. Added a note in the section “General Operating Condition”. 8. Updated the maximum values in the “LU Characteristics”

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Version	Date	Modifications
		table. 9. Updated the operating temperature range. 10. Updated the DNL and INL values in the section “ADC Electrical Characteristics”.
V1.3	Sep-20-2024	1. Updated the descriptions of “Communication interfaces”, “Analog Peripherals” and “Timers” on the home page. 2. Updated the ESD and LU electrical parameters on the home page. 3. Regarding “Table 1-1: Configuration Table”, modified the internal voltage reference of analog of UM32G421-HCU7 from “No” to “Yes”. 4. Updated some descriptions in “2.3.1 Embedded FLASH”. 5. Updated some descriptions in “2.9 DMA Controller”. 6. Updated some descriptions in “2.15 Timer / Counter (TIMx)”. 7. Regarding Table 4-5: Operating Condition at Power-up and Power-down, modified the maximum of t_{VDDH} from∞ to 20000. 8. Regarding Table 4-17: ESD Characteristics, modified the maximum of $V_{ESD(CDM)}$ from 2000 to 1500; and modified the standard compliance of $V_{ESD(HBM)}$ from “MIL-STD-883K Method 3015.9” to “ANSI/ESDA/JEDEC JS-001-2023”. 9. Regarding Table 4-18: LU Characteristics, modified the maximum of LU from 100 to 200. 10. Regarding Tables 4-20 and 4-21, modified the minimum value of “I/O Schmitt trigger voltage hysteresis” to a typical value. 11. Regarding Table4-22: ADC Electrical Characteristics, added corresponding values for single-ended and differential ENOB. 12. Regarding Table 4-24: OPA Characteristics, added the parameter SR, added “single-ended” to PGA mode. 13. Regarding Table 4-26: TS Characteristics, modified the maximum of T_L from ± 3 to ± 5. 14. Replaced the fonts and updated the formatting.
V1.3.1	Jan-20-2025	1. Regarding Table 3-2: Pin Description, modified the I/O structure of PB10 and PB11 from FT to Tta. 2. Regarding “Table 4-12: RCH Oscillator Characteristics” and

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Version	Date	Modifications
		"Table 4-13: RCL Oscillator Characteristics", modified the minimum of ACC_{RCH} and ACC_{RCL} from -1.5 to -2.5.
V1.3.2	Apr-21-2025	1. Updated Figure 4-1: Block Diagram of Power Supply Scheme. 2. Added the description "supporting incremental quadrature encoder and Hall sensor" for some timers. 3. Added the voltage noise density in Table 4-24: OPA Characteristics.
V1.3.3	Jul-10-2025	1. Updated Table 4-22: ADC Characteristics. 2. Added Table 4-23: ADC External Input Impedance Parameter. 3. Regarding Table 4-25: OPA Characteristics, modified the typical operating current value from 5 mA to 3 mA. 4. Added corresponding annotations to Figure 4-1: Block Diagram of Power Supply Scheme. 5. Updated the QFN32 package outline drawing and added the word "Reference" to the QFN48 package outline drawing.
V1.3.4	Aug-20-2025	1. Regarding Table 4-15: PLL Characteristics, modified the maximum values for both the VCO and PLL output clocks from 700 MHz to 600 MHz. 2. Updated package outline drawings for LQFP64, LQFP48, QFN40 and QFN32.
V1.3.5	Jan-26-2026	1. Added the external pin PC13 for Standby Mode 0 in Table 2-2: Low-power Modes Summary. 2. Updated the description of the main features in 2.12 Universal Synchronous / Asynchronous Receiver Transmitter (USART). 3. Updated the maximum CAN data rate. 4. Updated the maximum values for the VCO and PLL output clocks in Table 4-15: PLL Characteristics.
V2.0.0	Jul-13-2026	Updated the main frequency from 168 MHz to 204 MHz.

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